DEPARTMENT OF INSTRUMENTATION & CONTROL ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – Part I			
Session	**July – November, 2019**		
Course Title	**Circuit Theory (III Semester, 2018-22 batch)**		
Course Code	**ICPC 14**	**Credits**	**4**
Course Type	**Core**		
Pre-requisites	--		
Faculty	**Dr. Ramakalyan Ayyagari**	**Mobile No.** **Email**	**9443923485** **rkalyn@nitt.edu**
CC Chairman	**Dr. N. Sivakumaran**		
Other Course Teacher(s)/Tutor(s)	--		

SYLLABUS (approved in the BoS)

Review of Networks and Circuits, Elemental laws for Resistors, Inductors, and Capacitors, Kirchhoff's laws, Sign convention, Basic signals (dc and ac), Elementary signals, Synthesis of arbitrary waveforms from elementary signals, Voltage and Current sources, Ladder and Bridge Circuits.

Analysis of Resistive Circuits energized by dc voltages and currents –Source Transformations, Nodal and Mesh Analysis, Principle of Superposition, Network Theorems (Thevenin's and Norton's, Maximum Power Transfer), Circuits with dependent dc Sources.

Transients with Energy Storage Elements, First and Second Order Circuits –Time-constant, Damping Ratio, Natural Frequency, Emphasis on Linear Ordinary Differential Equations, Step response of RC, RL, and RLC (series and parallel) Circuits, Resonance in Second Order Circuits.

Sinusoidal Sources and Response –Behaviour of elements with ac signals, Impedance and Admittance, Generalization of Network Theorems and Circuit Analysis, Introduction to 3-ϕpower systems. Transient and Steady-state Response of Circuits –Laplace Transformation and its application to circuit analysis, State Variables, Network Functions, Transfer function, Two-port Networks, Applications of Two-port networks, Introduction to General Linear Systems.

Network Synthesis: Properties of RC, RL, and LC network functions, Synthesis of networks.

COURSE OBJECTIVES

To introduce and impart problem solving techniques, through linear passive electrical circuits, useful for other core and elective courses of the department.

To introduce algorithmic and computer-oriented methods for solving large scale circuits.

MAPPING OF COs With POs

Course Outcomes	Program Objectives
1. In unit I the student is motivated to study circuits in a systematic manner suitable for engineering analysis and design.	1,10, 12
2. In units II & III, the student understands formulating circuit analysis problems in a mathematically tractable way with an emphasis on solving linear systems of equations. Further, the student is exposed to subtle details in the responses of circuits subjected to sudden changes in excitation, and understanding the transient phenomena.	1,10, 12
3. In unit IV, the student understands the steady-state behaviour of circuits, generalization of ideas to complex exponential signals, and learns the basic principles of power systems	1,10, 12
4. In unit V, the student is goaded to understand circuit theory in a unified framework, learn about input-output modeling, and generalize the concepts to linear systems theory	1,10, 12

COURSE PLAN – Part II

COURSE OVERVIEW

The emphasis of this course is on the development of the basic ideas of electrical engineering, rather than on giving bland definitions. An additional objective of this course is to encourage the students to develop hierarchical thinking wherein they can see more complex systems as generalizations of simple circuits and techniques. There are no specific pre-requisites for this course; an understanding of elementary calculus and simple matrix methods is necessary and sufficient.

COURSE TEACHING AND LEARNING ACTIVITIES

Classes	Week(s)	Topic(s)	Mode of Delivery
1 – 4	July 25 – Aug 1	Introduction to the course	Board
5 – 16	Aug 5 – 9, 19 – 23, 26 – 30	Part I (DC Circuit Analysis)	Board/PPT
17 – 24	Sep 2 – 6, 9 – 13, 16 – 20	Part II (Transients)	Board/PPT
25 – 30	Sep 23 – 27, Sep 30 – Oct 4	Part III (AC Circuit Analysis)	Board/PPT
31 – 42	Oct 7 – 11, 14 – 18, 21 – 25	Part IV (s-domain Analysis)	Board/PPT
43 – 53	Oct 28 – Nov 1, Nov 4 – 8, 11 – 15	Part V (Network Synthesis)	Board/PPT

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Date	Duration	% Weightage
1 – 4	4 Assessments	Sep 6 Oct 11 Nov 1 Nov 15	60 minutes each	60%
5	Compensatory Assessment	Nov 13	60 minutes	15%
6	End-term Assessment Covering the entire syllabus	Nov 22		120 minutes

- **Evaluation will be completed by Nov 24 to facilitate Re-assessment on Nov 28 for students scoring < 35% or average/2, whichever is greater.**
- **Students can access their answer scripts, for the unlikely event of re-grading, on Nov 24**

RESULTS WILL BE SUBMITTED TO THE PAC ON November 29, 2019

BOOKS/LITERATURE:

1. Ramakalyan A., Linear Circuits: Analysis & Synthesis, Oxford Univ. Press, 2005.
2. W. Hayt & J.E. Kemmerley, Engineering Circuit Analysis, Tata McGraw Hill, 8/e, 2013.
3. Schaum's Outline Series, Electric Circuits, 6/e.

COURSE EXIT SURVEY

Feedback from the students during the class committee meetings
Feedback after Assessment 1 for mid-course correction
Feedback before End-term examination through a questionnaire, for improvements in future.

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

ATTENDANCE (REMEMBER THIS IS A 4-CREDIT COURSE)

- As per Rule B.4.5.2 (page 7, https://www.nitt.edu/home/academics/rules/BTech_Regulations_2018.pdf) 75% attendance, as on **November 15, 2019**, is mandatory, with an exemption up to 10% on genuine grounds; prior information and approval from the instructor is compulsory.
- The only option for students with attendance < 65% is RE-DO.

Assessments and Grading Policy

- A student can be, upon prior approval, absent from only one out of the the continuous assessments 1 – 4, for which he/she is allowed to take the compensatory assessment on November 11, 2019. Please note that compensatory assessment is not offered as an improvement test for everyone.
- A student is declared pass upon accumulating a minimum of 35% over all the 5 assessments; grading is done for those students declared passed based on the class average – average and above shall get S, A, and B grades, and below average shall get C, D, and E.
- In case one or more students fail to accumulate the stipulated minimum 35% (at the end of 5 assessments), they are permitted to take a one-time re-assessment for 100%; this is a 3-hour written examination on November 25, 2019, covering the entire syllabus.

Academic Honesty

- Mid-term and End-term assessments in this course must be strictly individual work.
- However, collaboration by individuals is encouraged at the level of ideas.
    - Feel free to ask each other questions, or brainstorm on solutions, or work together on a board. However, be careful about copying the actual solution. This sort of collaboration at the level of artifacts is permitted if explicitly acknowledged, but this is usually self-defeating.
- The principle behind the collaboration rule is simple:
    - I want you to learn as much as possible; you may learn from me or from each other.
    - The goal of artifacts (assessments) is simply to demonstrate what you have learned. So, I'm happy to have you share ideas, but if you want your own points you have to internalize the ideas and then craft them into an elegant solution by yourself, without any direct assistance from anyone else, and without relying on any idea taken from others (whether at this institute or from the web).

Academic Dishonesty

For purposes of this class, academic dishonesty is defined as:

- Any attempt to pass off work on a test that didn't come straight out of your own head.
- Any collaboration on artifacts in which the collaborating parties do not clearly explain exactly who did what, at turn-in time.
- Any activity that has the effect of significantly impairing the ability of another student to learn. Examples here might include destroying the work of others, interfering with their access to resources, or deliberately providing them with misleading information.

ADDITIONAL COURSE INFORMATION

All the students are urged to be interactive during the classes. Further, the students are suggested to make a google group for faster dissemination of PPTs, discussions etc. They are free to interact with me over email any time, and if needed meet me in person with prior appointment.

Any changes in the proposed layout of the semester, due to unavoidable circumstances, shall be intimated immediately to the students and to the Chairperson, PAC

FOR SENATE'S CONSIDERATION

Course Faculty	CC-Chairperson	HOD
26/7/19	26/7/19	27/8/19
Dr. Ramakalyan Ayyagari	Prof. N. Sivakumaran	Dr. B. Vasuki

ICPC 14 Circuit Theory

July – November 2019

Tue 8.30 am, Wed 9.20 am & Thu 10.30 am

Friday 11.20 is for Tutorials & Assessments

Jul 19 (3)	Aug 19 (13)	Sep 19 (12)	Oct 19 (17)	Nov 19 (9)
25 Regular class	1 Regular class	3 Regular class	1 Regular class	1 Regular class*
30 Regular class	6 Regular class	4 Regular class	3 Regular class	5 Regular class*
31 Regular class	7 Regular class	5 Regular class	4 Regular class	6 Regular class*
	8 Regular class	11 Regular class	9 Regular class	7 Regular class*
	13 Regular class	12 Regular class	10 Regular class	8 Regular class*
	14 Regular class	13 Regular class	11 Regular class	13 Regular class*
	20 Regular class	17 Regular class	15 Regular class	14 Regular class*
	21 Regular class	18 Regular class	16 Regular class	15 Regular class*
	22 Regular class	19 Regular class	17 Regular class	
	27 Regular class	24 Regular class	18 Regular class	
	28 Regular class	25 Regular class	22 Regular class	
	29 Regular class	26 Regular class	23 Regular class	
	30 Regular class		24 Regular class	
			25 Regular class	
			29 Regular class	
			30 Regular class	
			31 Regular class	

Last Regular Class, Attendance must be at least 75% as on this day

*Make-up/Review/Revision etc.

26/7/19

(Dr. Ramakalyan Ayyagari)

Course Instructor