DEPARTMENT OF Instrumentation and Control Engineering

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	B.Tech Instrumentation and Control Engineering		
Course Title	Analog Signal Processing Laboratory		
Course Code	ICLR13	No. of Credits	2
Course Code of Pre-requisite subject(s)	Nil		
Session	Jan 2019	Section (if, applicable)	A
Name of Faculty	Dr. S. Narayanan	Department	ICE
Email	narayanan@nitt.edu	Telephone No.	0431-2503364
Name of Course Coordinator(s) (if, applicable)	NA		
E-mail	------	Telephone No.	
Course Type	[√] Core course	[ ] Elective course	

Syllabus (approved in BoS)

List of experiments:

1. Design of amplifiers using various modes and its implementation issues
2. Filter design using various methodologies for different set of specifications
3. Sensor linearization and bridge linearization using op-amps
4. Design of waveform generators using op-amp
5. PLL design
6. Regulator design
7. Analog to digital conversion & digital to analog conversion
8. Regenerative feedback circuit design - Schmitt trigger and Multivibrator
9. Transmitter design

COURSE OBJECTIVES

1. To introduce system level design.
2. To impart knowledge in design and test Op-amp and other ICs based circuits.
3. To familiarize the students in simulation tools and evaluation boards available for analog signal processing.

COURSE OUTCOMES (CO)	
Course Outcomes	**Aligned Programme Outcomes (PO)**
At the end of the course, Students get enough exposure in the following skill sets. 1. Every experiment includes several features: pre-lab reading, theoretical analysis, result prediction at various nodes of the circuit. Experimental investigation, record keeping, data analysis, evaluation and inference.	
2. On completion of this lab, the students will be able to, 1. design circuits. 2. simulate and validate analog IC circuits using simulation software. 3. apply this basic IC circuit design concepts for application.	1,2,3,4,5,6,7

COURSE PLAN – PART II

COURSE OVERVIEW

The objective is to provide working practice in simulation tools & experiment test bench to learn the design and testing of various circuits (like amplifiers, filters, PLL and signal conditioning circuits) with digital and analog ICs.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	I	Op-Amp circuits with resistive feedback	Experiment
2	II	Filter design	Experiment
3.	III	Schmitt trigger & Precision rectifiers	Experiment
4.	IV	Multivibrators	Experiment
5.	V	Instrumentation Amplifier	Experiment
6.	VI	Waveform generators	Experiment
7.	VII	Phase Locked Loops	Experiment
8.	VIII	A/D and D/A converters	Experiment

9.	IX	Compensator circuits - Lead, Lag & PI	Experiment
10	X	Signal Conditioning Circuits	Experiment

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Simulation and Report	During every class	Pre-work and submission	15%
2	Experimentation and Report	During every class	Experimentation and submission	10% + 10%
3	Objective Test	During 6th Week	1 hour	20%
4	Desing problem test & Project	During 11th Week	2 hours with periodic review	30% + 15%

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**
- Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

FOR APPROVAL

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____