**DEPARTMENT OF INSTRUMENTATION AND CONTROL ENGINEERING**

***NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI***

# COURSE PLAN

| **COURSE OUTLINE** | | | |
|---|---|---|---|
| **Course Title** | **Digital Electronics** | | |
| **Course Code** | **ICPC 15** | **No. of Credits** | **3** |
| **Department** | **ICE** | **Faculty** | **Dr. D. Ezhilarasi** |
| **Pre-requisites Course Code** | **Nil** | | |
| **CourseTeacher Email** | **ezhil@nitt.edu** | **Mobile No.** | **9444878908** |
| **Course Type** | **Core course** | | |

## COURSE OVERVIEW

This course covers combinational and sequential logic circuits. Topics include number systems, Boolean algebra, logic families, medium scale integration (MSI) and large scale integration (LSI) circuits, analysis and design of combinational and sequential circuits. Upon completion, students should be able to construct, analyze, verify, and troubleshoot digital circuits using appropriate techniques and test equipment.

## COURSE OBJECTIVES

The subject aims to provide the student with
1) An understanding of number system, codes and their conversions
2) The capability to reduce Boolean expression using K-map and tabular methods
3) The ability to design and analyze combinational and sequential logic circuits for a given problem statement.
4) An understanding of Digital hardware and different types of logic families.

## COURSE OUTCOMES (CO)

Students will:
1.Understand how digital and logic computing is built from the fundamentals of semiconductor electronics and learn the capability to use abstractions to analyze and design digital electronic circuits
2. Gain knowledge on the basic logics and techniques related with digital computing
3. Develop expertise to design and implement various complicated digital systems to be applicable for signal measurement and processing

| **Course Outcomes** | **Aligned Programme Outcomes (PO)** |
|---|---|
| **1.** Understand how digital and logic computing is built from the fundamentals of | 1.would have developed an ability to apply the knowledgeof mathematics, sciences, and |

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|---|---|
| semiconductor electronics and learn the capability to use abstractions to analyze and design digital electronic circuits | engineering fundamentals to the field of instrumentation & control. |
| **2.** Gain knowledge on the basic logics and techniques related with digital computing | 2. would have possessed a comprehensive understanding of a wider range of electronic devices, analog and digital electronic circuits and the state-of-the-art advanced electronic systems invariably found in every measurement and instrumentation system |
| **3.** Develop expertise to design and implement various complicated digital systems to be applicable for signal measurement and processing | 3. would have recognized the need for engaging themselves in independent and life-long learning in the broadest context of technological change |

## COURSE TEACHING AND LEARNING ACTIVITIES

| S.No. | Weeks | Topic | Mode of Delivery |
|---|---|---|---|
| 1 | 1st & 2nd Week | Review of number systems and logic gates, Algebraic reductions, Binary codes -Weighted and non-weighted, number compliments, Binary arithmetic, Error detecting and error correcting codes | Chalk and talk |
| 2 | 3rd & 4th week | SOP, POS Canonical logic forms, Karnaugh maps and Quine-McClusky methods, Don't care conditions, minimization of multiple output functions.<br>Synthesis of combinational functions: Arithmetic circuits-Adder/Subtractor, carry look-ahead adder, signed number addition and subtraction, BCD adders. IC adders. | Chalk and talk |
| 3 | 5th & 6th week | Multiplexers, implementation of combinational functions using multiplexers, de-multiplexers, decoders, code converters, Digital ICs for combinational logic circuits, Complexity and propagation delay analysis of circuits. | Chalk & talk |
| 4 | 7th & 8th week | Sequential Logic: Basic latch circuit, Debouncing of a switch, Flip-Flops: truth table and excitation table, conversion of Flip-flops, integrated circuit flip-flops. Race in sequential circuits,. | Chalk and talk |
| 5 | 9th & 10th week | Shift Registers, Counters - Synchronous, Asynchronous, Up-Down, Design of counters<br>Analysis of clocked sequential circuits. | Chalk and talk |
| 6 | 11th & 12th week | Design with state equations, Moore and Mealy graphs, State reduction and assignment ,Sequence detection, Hazards. Programmable logic devices,Design using Programmable Logic Devices (ROM,PLA,PAL,FPGA). | Chalk and talk |
| 7 | 13th & 14th week | Digital Hardware: Logic levels, Digital integrated circuits, Logic delay times, Fan-Out and Fan-In, Logic families, Interfacing between different families. CMOS Electronics: CMOS electronics and Electronic logic gates, The CMOS inverter, Logic formation using MOSFETs, CMOS memories. | Chalk and talk |

## ESSENTIAL READINGS : Textbooks and reference books

1. M.M. Mano, Logic and Computer Design Fundamentals ,Pearson, 4thEdition, 2014
2. J.P. Uyemura, A First Course in Digital Systems Design, Brooks/Cole Publishing Co.
3. W. H. Gothmann, "Digital Electronics - An Introduction to Theory and Practice", Prentice Hall of India, 2000
4. Ronald J. Tocci, Digital Systems- Principles and Applications,10th Edition, Pearson International, 2007
5. J.M. Rabaey, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall of India, 2003

## COURSE ASSESSMENT METHODS

| S.No. | Mode of Assessment | Week/Date | Duration | % Weightage |
|---|---|---|---|---|
| 1 | Hands on Test -1 | Third Week of August | 1 hour | 15% |
| 2 | Test-2 | First Week of October | 1 1/2Hour | 25% |
| 3 | Assignment | Forth week of October | | 10% |
| 4 | End Sem Exam | Second Week of December | 3 Hours | 50% |

## COURSE EXIT SURVEY

Written feedback from students during middle of the course

## COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

Retest will be conducted for students who miss Test1 or Test2. But they should get permission from the faculty by giving valid reason in written form to write retest.

65 % attendance is must. Below 65 % attendance will be awarded V Grade (Redo)

**Grading Policy**
Relative grading based on normalized curve or Z-score will be followed
**Reassesment Examination**

- A student may, for valid reasons on production of valid medical certificate and with the approval of Head of the Department be permitted to withdraw from appearing for the End Sem Examination. Withdrawal application shall be valid only if it is made before the commencement of the examination.
- For students who miss the final sem assessment, reassessment will be conducted for 50% mark and internal marks remain same.
- Those who failed in the subject may register for reassesment examination which will be conducted for 100% mark (Absolute grading where passing minimum is 40).
- Grades for the students who have withdrawn from writing the end sem exam will be same as the regular assessment grades. For those who are failed or absent and

appearing for reassessment, the maximum grade is restricted to 'E'.

- Reassesment exam will be conducted in the first week of the next semester or earlier during the vacation.
- Students who fail in reassesment exam have to register for formative assessment.

## ADDITIONAL COURSE INFORMATION

The Course instructor is available for consultation at any time during office hours.
Queries may also be emailed to the Course instructor directly at ezhil@nitt.edu

## FOR SENATE'S CONSIDERATION

**Course Faculty** 27/7/17.

**CC-Chairperson** Goldin R. Bennet 27/7/2017

**HOD** 27/7/17

**Date:** 27-7-2017

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