DEPARTMENT OF INSTRUMENTATION AND CONTROL ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN

COURSE OUTLINE				
Course Title	CIRCUIT THEORY - (III semester 'B' Section)			
Course Code	ICPC14	No. of Credits	4	
Department	ICE Department	Faculty	Dr. K. Srinivasan	
Pre-requisites				
Course Coordinator	None			
E-mail	srinikkn@nitt.edu	Telephone No	0. 0431-2503363	
Course Type	Core course			

COURSE OVERVIEW

This is the fundamental course. The student can able to analyze and synthesis the linear, passive circuit components.

COURSE OBJECTIVES

- To introduce and impart problem solving techniques, through linear passive electrical networks, useful for othe core and elective courses of the department.
- To introduce algorithmic and computer oriented methods for solving large scale circuits.

COURSE OUTCOMES (CO)

- The student can able to solve DC circuit analysis using network theorem and transient analysis of linear passive networks.
- The student can familiar with AC circuit analysis using network theorem and frequency response analysis of linear passive networks.
- The student can able to analyse different two port network and network synthesis using Foster and cauer forms.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No. We	ek Topic	Mode of Delivery
1. First wee	Review of networks and circuit, Elemental laws (V I characteristi Resistors , Inductors and Capacit Circuitral laws (Kirchhoff's laws) mesh analysis.	tors,

2.	Second week	Mesh and Nodal analysis, Analysis of Resistive circuits energized by DC voltage and current – Source	Black/ white board
		transformations. Introduction to Network theorems.	Paperson Sylvin Mag
3.	Third week	Principle of Superposition and Thevinin's theorem	Black/ white board
4.	Fourth week	Norton's theorems, Maximum power transfer theorem, Circuits with dependant dc sources.	Black/ white board
5.	Fifth week	Transients with energy storage element, (RC and RL electrical circuit)	Black/white board
6.	Sixth week	Introduction to RL and second order RLC circuits	Black/white board
	Sixth week	Assessment −1: Written exam (20% Weightage)	Course outcome – 1
7.	Seventh week	Transient response analysis of RLC circuit (Series and Parallel)	Black/white board
8.	Eighth week	Resonance in second order circuit and dependent source problem.	Black/white board
	Eigth week	Assessment -2 : (15% Weightage)	Course outcome – 1 8
9.	Nineth week	Sinusoidal sources and response- Behaviour of elements with ac signals, Impedance and admittance, Generalization of network theorems and circuit analysis.	Black/white board Power point presentation
10.	Tenth week	Transient and steady state response of circuits. Network functions (Driving point	Black/white board Power point presentation

		impedance and admittance), Transfer function, Two port networks.	and the state of the second
11.	Eleventh week	Applications of two port networks, Introduction to general linear system. state variables analysis	Black/white board Power point presentation
12.	End of 11 th week	Assessment -3: Written exam (20% Weightage)	Course outcome -3
13.	Twelveth week	Network synthesis: Properties of RC,RL and RLC driving point functions.	Black/white board Power point presentation
14.	Thirteenth week	Synthesis of networks from given transfer function using Foster and cauer forms.	Black/white board Power point presentation
15.	End of 13 th week	Assessment -4: (15% Weightage)	Course outcome- 2 & 3
16.	End of 14 th week	Assessment -5: Written exam (30% Weightage)	Course outcome-1,2 &3
17.	End of 15 th week	Reassessment	Course outcome-1,2 & 3

COURSE ASSESSMENT METHODS

S.No.	Assessment ·	Week/Date	Duration	% Weightage
1.	Assessment -1 Written exam -1	End of 6 th week	One hour	20%
2.	Assessment 2 Assignment - I (problem solving and validation using simulation software)	End of 8 th week	-	15%
3.	Assessment -3 Written exam -2	End of 11 th week	One hour	20%
4.	Assessment -4 Assignment - II (problem solving and validation using simulation software)	End of 13 th week	<u>.</u>	15%
5.	Assessment -5 Written exam-3	End of 14 th week	Two hour	30%
6.	Reassessment Written (2 Hour) for 70% plus Assignments for 30%	End of 15 th week	Two Hour	100%

ESSENTIAL READINGS: Textbooks, reference books Website addresses, journals, etc.

- 1. Hayt W.H, Kemmerly J.E, & Durbin, Engineering circuit analysis, Mc Graw Hill Publications, 8th edition, 2013.
- 2. Ramakalyan, A., Linear Circuits: Analysis and Synthesis, Oxford University press 2005.
- 3. Van Valkenburg, M.E., Introduction to modern network synthesis, Wiley 1960.
- 4. Van Valkenburg, M.E., network Analysis Prentice Hall,3rd Edition,2006.
- D Roy Choudhury, Networks and Systems New age International publishers, 2nd Edition, 2010.
- 6. John O'.Malley schaum's outline of Theory and Problems of Basic circuit analysis 2nd Edition,1992.

COURSE EXIT SURVEY

- 1. Exit survey through questionnaire at the end of course.
- 2. Direct feedback from the students.
- 3. Feedback from the students during the class committee meetings.

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

All students are expected to do their own work. The taking of information by means of copying homework assignments, or looking or attempting to look at another student's paper during an examination is considered dishonest. The tendering of information, such as giving your work to another student to be used or copied is also considered dishonest.

Also, preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.

Any evidence of such academic dishonesty will result in the loss of all marks on that assessment. Additionally, the names of those students so penalized will be reported to the Office of Dean (Students) and the Office of Dean (Academic) for the records.

Attendance Policy:

- 1. 80% attendance is mandatory. In case the student is having attendance between (65-80)%, the students can compensate it by reporting class teacher and solving problems covered on syllabus for the syllabus on absentee days. The revised attendance for the student before end of semester should be 80%.
- 2. However if the student got less than 80% even after compensation they have to redo the course.

Assessemnt Policy:

- 3. After the regular assessments are completed, provisional results will be displayed. Those who are shown with less than 35% in the provisional result, will have to appear for reassessment exam to pass the course in second attempt.
- 4. Any student absent for any assessment due to any genuine reason will have to appear for reassessment written exam. The exam will be conducted on the entire syllabus. The duration of the exam is 2 hours. If the student absents for more than one assessment, other assessment marks will be awarded as zero.
- 5. Relative grading will be followed for awarding the grades. However the passing minmum for the award of E grade should be 35%.

- 6. The re assessment test will be 100% (70% weightage for 2 hour Written exam and 30% weightage for Assignment). In case if the student fails in reassessement (less than 35%), the student has to register under formative assessment only. If the student got more than 35%, he will be awarded as 'E' Grade.
- 7. The Assessment date and time will be fixed by the faculty in consultation with class representative as per the evaluation schedule.

General Policy:

- 8. 100% Transparency will be maintained in all the evaluations. The answer script will be shown to the students immediately after evaluation. Any discrepancy in evaluation should be reported immediately to the faculty member and it will be sorted out immediately. The student should strictly adhere the time window for inspection of the evaluated answer scripts.
- **9.** After final allocation of the grades after the reassessment exam, the grades will be uploaded in the MIS and it will be forwarded to the Academic Office.
- 10. Students opting for plagiarism during exams will be summarily sent out and awarded zero marks for that exam.
- 11. Students honestly producing original work will be rewarded with better marks.

ADDITIONAL COURSE INFORMATION

Students can meet any time depends on their mutual availability.

Any suggestions, Queries and feedback can be emailed to the Course Coordinator directly at srinikkn@nitt.edu.

14/7/2017

Poldin R. Bennet
18-7-2017

FOR SENATE'S CONSIDERATION

Course Faculty

CC-Chairperson

HOD bymingle

Date: 18-7-2017

National Institute of Technology