DEPARTMENT OF INSTRUMENTATION & CONTROL ENGINEERING NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

Cours	e Title	Circuit Theory					
Course Code		ICPC 14	Credits	3			
Depar	tment	ICE, III Semester Section A	Faculty	Dr. Ramakalyan Ayyagari			
Pre-re	quisites						
Other	Course		Mobile No.	+919443923485			
Teacher(s)/Tutor(s)		Email		rkalyn@nitt.edu			
Course Type		PROGRAM CORE		**************************************			
COUR	SE OVERVIEW						
The e	mphasis of this	course is on the development	of the basic id	eas of electrical engineering			
		bland definitions. An additiona		그리다 가는 사람이 있다면 하는 것이 되었다면 하는 것이 없는 것이 없는 것이 없는 것이 없는 것이 없는데 없다.			
		hierarchical thinking wherein					
		mple circuits and techniques.					
		nding of elementary calculus a	nd simple matr	ix methods is necessary and			
suffici							
	SE OBJECTIVES						
		impart problem solving techniq		ear passive electrical circuits			
		ore and elective courses of the					
		lgorithmic and computer-orien	ted methods fo	r solving large scale circuits.			
COUR	SE OUTCOMES						
		e course, the student is motiva					
1.	suitable for	engineering analysis and d	esign. Further,	the student understand			
1.	formulating c	ircuit analysis problems in a ma	thematically tra	ctable way with an emphasi			
	on solving line	ear systems of equations.					
		Alignment with the Program	Outcomes: 1,	10, 12			
	In part II, the	student is exposed to subtle de	tails in the resp	onses of circuits subjected to			
2.		ges in excitation, and understan					
		Alignment with the Program	Outcomes: 1,	10, 12			
	In part III, the student understands the steady-state behavior of cirucits, generalization o						
3.	ideas to complex exponential signals. Further he is goaded to understand circuit theory is a unified framework, learn about input-output modeling, and generalize the concepts to						
	linear systems theory - Control Systems, and Communication Systems.						
		Alignment with the Program					
	In part IV, the	student is goaded to understan	d circuit theory	in a unified framework, learn			
4.	about input-output modeling, and generalize the concepts to linear systems theory						
	Control Systems, and Communication Systems.						
	control o you	Alignment with the Program		10. 12			
	In part V, the						
5		he student is introduced to the design of networks, given certain specifications					
5.		nd/or constraints, with a good balance of intuiton developed in the earlier parts, and athematical rigour.					
	mathematica	Leigoue					
		rigour. Alignment with the Program	Outcomes: 1,	10, 12			

Classes	Dates	Topic(s)	Mode of Delivery
1-2	July 10, 11	Introduction to the course	Board
3 – 12	July 17, 18, 20, 24, 25, 27, 31, Aug 1	Part I (DC Circuit Analysis)	Board/PPT
	August 3: ASSESSMENT 1: 1	nour test for 15% weight, coveri	ng Part I
13 - 18	Aug 7, 8, 10, 17	Part II (Transients)	Board/PPT
19 – 24	Aug 21, 22, 24, 28, 29	Part III (AC Circuit Analysis)	Board/PPT
	August 31: ASSESSMENT 2: 1 hou	ur test for 15% weight, covering	Parts II & III
25 - 36	Sep 4, 5, 7, 11, 12, 14, 18, 19, 21	Part IV (s-domain Analysis)	Board/PPT
	September 25: ASSESSMENT 3:	1 hour test for 15% weight, cove	ering Part IV
37 – 44	Sep 26, Oct 3, 5, 9, 10, 12	Part V (Network Synthesis)	Board/PPT
		hour test for 15% weight cover	ing Part V

October 26: ASSESSMENT 4: 1 hour test for 15% weight, covering Part

A detailed course calendar is attached herewith.

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Date	Duration	% Weightage
1-4	4 Assessments	Aug3, Aug 31, Sept 25, Oct 26	60 minutes each	60%
5	Compensatory Assessment	Oct 30	60 minutes	15%
6	End-term Assessment Covering the entire syllabus	Nov 2	120 minutes	40%
7	Re-assessment Covering the entire syllabus	Nov 11	180 minutes	100%

- Evaluation will be completed by Nov 6 to facilitate Re-assessment on Nov 11 for students scoring < 35%.
- Students can access their answer scripts, for the unlikely event of re-grading, on Nov 6

RESULTS WILL BE SUBMITTED TO THE PAC ON November 7, 2017

ESSENTIAL READINGS:

- 1. Ramakalyan A., Linear Circuits: Analysis & Synthesis, Oxford Univ. Press, 2005.
- 2. W. Hayt & J.E. Kemmerley, Engineering Circuit Analysis, Tata McGraw Hill, 8/e, 2013.
- 3. Schaum's Outline Series, Electric Circuits, 6/e.

COURSE EXIT SURVEY

Feedback from the students during the class committee meetings

Feedback before End-term examination through a questionnaire, for improvements in future.

COURSE POLICY (including attendance, grading, academic honesty, etc.)

ATTENDANCE

100% attendance, as on October 12, 2017, is mandatory, with an exemption up to 20% on genuine grounds; prior information and approval from the instructor is compulsory. • The only option for students with attendance < 80% is RE-DO.</p>

ASSESSMENTS AND GRADING POLICY

A student can be, upon prior approval, absent from only one out of the the continuous assessments 1 - 4, for which he/she is allowed to take the compensatory assessment on October 30, 2017. Please note that compensatory assessment is not offered as an improvement test for everyone.

- A student is declared pass upon accumulating a minimum of 35% over all the 5 assessments; grading is done for those students declared passed based on the class average – average and above shall get S, A, and B grades, and below average shall get C, D, and E.
- In case one or more students fail to accumulate the stipulated minimum 35% (at the end of 5 assessments), they are permitted to take a one-time re-assessment for 100%; this is a 3hour written examination on November 11, 2017, covering the entire syllabus.

ACADEMIC HONESTY

- Mid-term and End-term assessments in this course must be strictly individual work.
- However, collaboration by individuals is encouraged at the level of ideas.
 - Feel free to ask each other questions, or brainstorm on solutions, or work together on a board. However, be careful about copying the actual solution. This sort of collaboration at the level of artifacts is permitted if explicitly acknowledged, but this is usually self-defeating.
- The principle behind the collaboration rule is simple:
 - o I want you to learn as much as possible; you may learn from me or from each other.
 - The goal of artifacts (programs) is simply to demonstrate what you have learned. So, I'm happy to have you share ideas, but if you want your own points you have to internalize the ideas and then craft them into an artifact by yourself, without any direct assistance from anyone else, and without relying on any idea taken from others (whether at this institute or from the web).

ACADEMIC DISHONESTY

For purposes of this class, academic dishonesty is defined as:

- Any attempt to pass off work on a test that didn't come straight out of your own head.
- Any collaboration on artifacts in which the collaborating parties do not clearly explain exactly who did what, at turn-in time.
- Any activity that has the effect of significantly impairing the ability of another student to learn. Examples here might include destroying the work of others, interfering with their access to resources, or deliberately providing them with misleading information.

ADDITIONAL COURSE INFORMATION

All the students are urged to be interactive during the classes. Further, the students are suggested to make a google group for faster dissemination of PPTs, discussions etc. They are free to interact with me over email any time, and if needed meet me in person with prior appointment.

Any changes in the proposed layout of the semester, due to unavoidable circumstances, shall be intimated immediately to the students and to the Chairperson, PAC

FOR SENATE'S CONSIDERATION

Course Faculty

alamos,

Dr. Ramakalyan Ayyagari

CC-Chairperson

Prof. G.R. Bennet

HOD

Dr. B. Vasuki

