DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	**B.Tech. ELECTRICAL AND ELECTRONICS ENGINEERING**		
Course Title	**DIGITAL SYSTEM DESIGN AND HDLs**		
Course Code	**EEPC18**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**-**		
Session	**Jan 2021 (Re-Do)**	**Section (if, applicable)**	**-**
Name of Faculty	**Dr. S. Moorthi**	**Department**	**EEE**
Email	**srimoorthi@nitt.edu**	**Telephone No.**	**0431-2503267**
Name of Course Coordinator(s) (if, applicable)	**-**		
Course Type	☐ **Core course** ☑ **Elective course**		

Syllabus (approved in BoS)

Finite State machines - Mealy and Moore, state assignments, design and examples – Asynchronous finite state machines – design and examples – multi-input system controller design.

Programmable Devices: Simple and Complex Programmable logic devices (SPLD and CPLDs), Field Programmable Gate Arrays (FPGAs), Internal components of FPGA, Case study: A CPLD and a 10 million gates type of FPGA.

VHDL- Modeling styles – structural – Behavioral – Dataflow - Design of simple/ complex combinational and sequential circuits using VHDL – Data types – Test bench and simulation. Case study on system design.

Verilog HDL - Modeling styles – structural – Behavioral – Dataflow - Design of simple/ complex combinational and sequential circuits using Verilog – Test bench and simulation – case study on system design.

Fault classes and models – Stuck at faults, Bridging faults - Transition and Intermittent faults. Fault Diagnosis of combination circuits by conventional methods - Path sensitization technique – Boolean different method and Kohavi algorithm.

Text Books:

1. William I. Fletcher, 'An Engineering Approach to Digital Design', Prentice Hall, 2009.
2. Donald D.Givone, 'Digital Principles and Design', Tata McGraw-Hill, 1st Edition, 2003.
3. Morris Mano, 'Digital Design', PHI, 3rd Edition, 2005.
4. J. Bhaskar, 'Verilog HDL Primer', BPB publications, 2000.

Reference Books:

1. Samuel C. Lee, 'Digital Circuits and Logic Design', PHI Learning, 1st Edition, 2008.

COURSE OBJECTIVES	
To impart the concepts of Digital Systems and Hardware Description Languages.	
COURSE OUTCOMES (CO)	
Course Outcomes	**Aligned Programme Outcomes (PO)**
1. To understand the insights of the finite state machines.	PO1, PO2, PO3, PO6, PO8, PO9, PO10, PO13.
2. To appreciate and classify the programmable logic devices and FPGA.	
3. To design the logic circuits using VHDL.	
4. To develop the systems using Verilog HDL.	
5. To test the circuits for different faults.	

COURSE PLAN – PART II			
COURSE OVERVIEW			
This is a second level course next to Digital Electronics which deals with the design of finite state machines and controllers with its subsequent implementation using Hardware Description Languages like VHDL and Verilog HDL. In addition, different faculties and the testing methods in digital circuits are included.			
COURSE TEACHING AND LEARNING ACTIVITIES			
S.No.	**Week/Contact Hours**	**Topic**	**Mode of Delivery**
1.	1 (two contact hours)	Review of Digital fundamentals	C&T
2.	1 (one contact hour), 2, 3 (two contact hours)	Finite State machines - Mealy and Moore, state assignments, design and examples – Asynchronous finite state machines – design and examples – multi-input system controller design	C&T, PPTs (partly Flip-class)
3.	3 (one contact hour)	*Objective Test*	-
4.	4 (two contact hours)	Simple and Complex Programmable logic devices (SPLD and CPLDs)	PPT (Flip-class)
5.	4 (One contact hour)	Design problems in PLDs	PPT
6.	5 (two contact hours)	Field Programmable Gate Arrays (FPGAs), Internal components of FPGA.	PPT (Flip-class)
7.	5 (one hour), 6	Guest Lecture about recent FPGAs from company.	PPT, C&T
8.	7 (two hours)	VHDL- Modeling styles – structural – Behavioral – Dataflow.	C&T, PPT
9.	7 (one hour), 8, 9	Design of simple/ complex combinational and sequential circuits using VHDL.	C&T, PPT (Flip-class)
10.	10 (two hours)	Data types – Test bench and simulation.	C&T,PPT (Flip-class)
11.	10 (one hour), 11 (one hour).	*Design and Simulation test*	
12.	11 (one hour)	*Assignment 1: Case study on system design using VHDL.*	

13.	**11 (one hour), 12**	**Verilog HDL - Modeling styles – structural – Behavioral – Dataflow - Design of simple/ complex combinational and sequential circuits using Verilog, Testbench and Simulation.**	**C&T, PPT (partly Flip-class)**
14.	**13 (one hour)**	*Assignment 2: case study on system design using Verilog HDL.*	
15.	**13 (one hour)**	**Fault classes and models – Stuck at faults, Bridging faults - Transition and Intermittent faults.**	**C&T, PPT and VC**
16.	**13 (one hour), 14**	**Fault Diagnosis of combination circuits by conventional methods - Path sensitization technique - Boolean different method and Kohavi algorithm**	**C&T, PPT and VC**
17.	**14 (one hour)**	*Compensation Assessment (CPA)*	
		Final Written Exam	

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	**Objective Test**	**3**	**One hour**	**20**
2	**Design & Simulation Test**	**6**	**One hour**	**20**
3	**Assignment Evaluation**	**9**	**-**	**10**
CPA	*Compensation Assessment**	*16*	*One hour*	*20*
4	**Final Assessment**	**End of semester**	**Three hours**	**50**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire
End semester feedback on Course Outcomes

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)

1. **All the students are advised to check their WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail only.**
2. **Queries (if required) to the course teacher shall only be emailed to digital.eee.nitt@gmail.com**

COMPENSATION ASSESSMENT POLICY

1. **Attending all the assessments are MANDATORY for every student.**
2. **If any student is not able to attend any of the continuous assessments CAs: 1 (refer Sl. Nos. in course assessment methods) due to genuine reason, student is permitted to attend the compensation assessment (CPA) with % weightage equal to maximum of the CAs. However, maximum of the % weightage among the assessments for which the student was absent will be considered for computing marks for CA.**
3. **At any case, CPA will not be considered as an improvement test.**
4. **The minimum marks for passing this course and grading pattern will adhere to the regulations of the Institute.**

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **Attending all the classes for this course is mandatory.**
- **Attendance policy will be as per the Institute's regulation for the Online classes.**

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

  The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

The Course Coordinator is available for consultation at times that is displayed on the coordinator's office notice board.

Queries may also be emailed to the Course Coordinator directly at digital.eee.nitt@gmail.com

FOR APPROVAL

Course Faculty _____ 3/6/2021 **HOD** _____