DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	**B.Tech. (CSE)**		
Course Title	**Elements of Computing Systems**		
Course Code	**CSIR15**	**No. of Credits**	**2**
Course Code of Pre-requisite subject(s)	**------**		
Session	**July 2018**	**Section (if, applicable)**	**A & B**
Name of Faculty	**Dr. S. Mary Saira Bhanu**	**Department**	**CSE**
Email	**msb@nitt.edu**	**Telephone No.**	**9442970006**
Name of Course Coordinator(s) (if, applicable)	**-------NA------**		
E-mail		**Telephone No.**	
Course Type	**Core course**		

Syllabus (approved in BoS)

CSIR15 Elements of computing systems (Branch specific course)

Unit – I Concept-Program-Input-Processing-Output

Demo of simple high level language program to low level machine level language program tracing their execution from high level to circuit level/ gate level - Overview of the Hardware Description Language (HDL) - Designing a set of elementary logic gates from primitive NAND gates.

Design of binary adders, culminating in the construction of a simple ALU (Arithmetic-Logic Unit) using logic gates - Design of memory hierarchy from elementary flip-flop gates to registers and RAM units of arbitrary sizes using logic gates

Unit – II Introduction to Low level language

Introducing an instruction set, in both binary and assembly (symbolic) versions; Writing some low-level assembly programs - Other details of computer architecture - Basic language translation techniques: parsing, symbol table, macro-assembly

Unit – III Introduction to Virtual Machine

The role of virtual machines in modern software architectures like Java and .NET; Introduction of a typical VM language, focusing on stack-based arithmetic, logical, and memory access operations - VM abstraction and implementation, focusing on stack-based flow-of-control and subroutine call-and-return techniques

Unit – IV Introduction to Compilers

Context-free grammars and recursive parsing algorithms; Building a syntax analyzer (tokenizer and parser) The syntax analyzer to generate XML code reflecting the structure of the translated program - Code generation, low-level handling of arrays and objects

Unit – V Introduction to OS

Discussion of OS/hardware and OS/software design trade-offs, and time/space efficiency considerations - Design and implementation of some classical arithmetic and geometric algorithms for the implementation of OS - memory management, string processing, and I/O handling algorithms

Text Book

1. Noam Nisan, Shimon Schocken, "The Elements of Computing Systems: Building a Modern Computer from First Principles", The MIT Press, 2005

COURSE OBJECTIVES

- To make the student understand the basic building blocks of a computing system
- To make the student understand the flow of Concept-Program-Input-Processing-Output
- To introduce low level language, translators, operating system

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned Programme Outcomes (PO)**
1. Ability to trace the Concept-Program- Input-Processing- Output	**PO1, PO3, Po7O**
2. Ability to generate low level code for simple programs	**PO1, PO3, PO6, PO7**
3. Ability to design simple arithmetic and memory units	**PO1 - PO7**

COURSE PLAN – PART II

COURSE OVERVIEW

This course deals with designing, developing and building hardware and software systems. It helps the students to understand the working of computers at the hardware level. Also it describes the role of assemblers, compilers and operating systems in program execution.

COURSE TEACHING AND LEARNING ACTIVITIES			
S.No.	**Week/**	**Topic**	**Mode of Delivery**
1	1	Introduction to computing- Languages- High level language – Low level language – Steps to execute an instruction- Introduction to Computer Architecture, Stored program concept – Von Neumann model – Processing unit- memory – Input and output – control unit- - Tracing of program execution from high level to Hardware level	C & T
2	**2**	Hardware – Boolean Algebra - Boolean Logic, Boolean Functions, Gate Logic - Overview of HDL – Comparison of Verilog and VHDL - Designing elementary gates using HDL. Overview of Hardware Simulator downloaded from www.nand2tetris.org	C &T , PPT
3	**3**	Introduction to Combinational circuit and designing basic gates, arithmetic circuits multiplexers, demultiplexers, using hardware simulator	C & T, PPT
4	**4**	Introduction to sequential circuits, Designing elementary flip flops, registers and RAM units using hardware simulator	C & T, PPT
5	**5**	Introduction to Low level Language - Data representation- Processor, memory, registers abstractions, machine language, assembly language, Instruction Set Architecture- Instruction sets, addressing modes	C & T

6	**6**	Machine language Specification – use of Hack computer – A and C instruction of hack platform- Symbols – input/output handling - If logic and While Logic- Microoperation- Three address code generation	C & T , PPT
7	**7**	Introduction to assembly language programming – Assemblers- types of assemblers- writing simple programs	C &T
8	**8**	Assembler implementation – Parser – code- symbol table – macro assembly - two pass assemblers. Overview of Hack assembler	C&T, PPT
9	**9**	Introduction to virtual machine - Virtual machine paradigm – Stack machine model - Stack based arithmetic	C &T
10	**10**	Logical, and memory access operations using stack - Implementation of Virtual machine translator- Working of Java virtual Machine	C &T
11	**11**	Program control - usage of subroutines Implementation of function call and return, Overview of VM emulator	C&T, PPT
12	**12**	Introduction to compilers – context free grammars – Parsing – Phases of Compilers	C & T
13	**13**	Implementation of Syntax analyzer - Implementation of tokenizer, Parser, Code generation – Data translation – Handling variables, arrays, objects- Compilation process	C & T
14	**14**	Introduction to OS –Components of OS - Process Management – Implementation of arithmetic operations at the OS level- Memory management – Memory allocation algorithms	C & T

15	**15**	Input / Output management Graphics output, character output, Keyboard Handling	C & T

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Written Test 1	September IV week	1 hour	20
2	Assignment	October IV Week		10
3	Written Test 2	November II week	1 hour	20
CPA	Compensation Assessment*	December First Week		20
4	Final Assessment *	December Third Week	3 hours	50

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback to be collected at the end of semester through MIS

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)
Through email
COMPENSATION ASSESSMENT POLICY
Students should not absent for assessments. If the reason for absence is genuine, the student can appear for compensation assessment. The medical certificate/on duty certificate should be submitted within one week after rejoining. The portions for the compensation assessment will be Test 1 and Test 2 portions.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**
- Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

FOR APPROVAL

Course Faculty _____ CC-Chairperson _____ HOD _____

Guidelines:

a) The number of assessments for a course shall range from 4 to 6.

b) Every course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) **One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered. Details of compensation assessment to be specified by faculty.**

d) The passing minimum shall be as per the regulations.

e) Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

f) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

g) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.