NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE PLAN – PART I			
Name of the programme and specialization	B.Tech- EEE		
Course Title	VLSI DESIGN		
Course Code	EEPC24	No. of Credits	3
Course Code of Pre-requisite subject(s)	EEPC15, EEPC17		
Session	January 2020	Section (if, applicable)	A
Name of Faculty	Mr. K. R. Pasupathy	Department	ECE
Official Email	pasupathy@nitt.edu	Telephone No.	8754471441
Name of Course Coordinator(s) (if, applicable)			
Official E-mail		Telephone No.	
Course Type (please tick appropriately)	Core course ✓	Elective course	

Syllabus (approved in BoS)

- MOS characteristics: NMOS characteristics, inverter action – CMOS characteristics, inverter action -models and second order effects of MOS transistors – Current equation – MOSFET Capacitances -MOS as Switch, Diode/ resistor – current source and sink – Current mirror.
- CMOS Fabrication – n-well, p-well, twin-tub processes – fabrication steps – crystal growth – photolithography – oxidation – diffusion – Ion implantation – etching – metallization.
- CMOS Logic Circuits: Implementation of logic circuits using nMOS and CMOS, Pass transistor and transmission gates – Implementation of combinational circuits – parity generator – magnitude comparator – stick diagram – layout design.
- Memory design – SRAM cell – 6T SRAM – DRAM – 1T, 3T, 4T cells, CMOS Sequential circuits: Static and Dynamic circuits – True Single-phase clocked registers – Clocking schemes.
- ASIC - Types of ASICs - Design flow – Design Entry – Simulation – Synthesis – Floor planning –Placement – Routing - Circuit extraction – Programmable ASICs.

COURSE OBJECTIVES

To enrich the student with the concepts of VLSI devices and its fabrication and also to develop Different electronic circuits.

MAPPING OF COs with Pos

Course Outcomes	Programme Outcomes

	(PO)
Upon completion of the course the students would be able to	
1. To understand the insights of the MOS devices and its characteristics.	2,7,9,13
2. To appreciate the different VLSI process technologies.	3,8,10
3. To design the CMOS combinational logic circuits and its layout.	2,3,8,14
4. To develop the sequential circuits and clocking schemes.	2,3,8,10,14
5. To realize the Design flow of application-specific Integrated circuit.	4,8

COURSE PLAN – PART II

COURSE OVERVIEW

This course provides the knowledge about NMOS, and CMOS technologies. Students will be able to learn about Programmable memory design and able to design different ASIC & FPGA. They can acquire knowledge of fabrication of IC's and types of CMOS logic circuits.

8COURSE TEACHING AND LEARNING ACTIVITIES

S.No	Week/Contact Hours	Topic	Mode of Delivery
1.	Week 1 06-10 Jan 2020 (3 Contact hour)	VLSI – Historical Perspective, Moore's law, Downsizing, MOSFET – structure, MOS operation, MOSFET working, MOSFET characteristics.	Chalk & Talk
2.	Week 2 13-17 Jan 2020 (1 Contact hours)	Drain current derivation, Threshold voltage expression.	Chalk & Talk
3.	Week 3 20-24 Jan 2020 (3 Contact hours)	Second order effects. MOSFET capacitances, MOS as switch, Diode/resistor – current source and sink – current mirror.	Chalk & Talk
4.	Week 4 27-31 Jan 2020 (2 Contact hour)	CMOS Inverter action and characteristics	Chalk & Talk
5.	Week 5 3-7 Feb 2020 (3 Contact hours)	CMOS Fabrication – nwell, p-well, twin-tub processes.	PPT
6.	Week 6 10-14 Feb 2020 (3 Contact hours)	Fabrication steps-crystal growth-photolithography-oxidation, Diffusion.	PPT
7.	Week 7 17-21 Feb 2020 (1+2 Contact hours)	**ASSESSMENT 1** Ion implantation-etching-metallization. CMOS Logic circuits :	Chalk & Talk/PPT

		implementation of logic circuits using nMOS and CMOS.	
8.	Week 8 24-28 Feb 2020 (3 Contact hour)	Pass transistor and transmission gates. Implementation of combinational circuits – parity generator	Chalk & Talk
9.	Week 9 2-6 March 2020 (3 Contact hours)	Magnitude comparator. Stick diagram and layout design. Memory design – SRAM cell – 6T SRAM.	Chalk & Talk/PPT
10.	Week 10 9-13 March 2020 (1 Contact hours)	DRAM – 1T, 3T, 4T cells.	Chalk & Talk
11.	Week 11 16-20 March 2020 (3 Contact hours)	CMOS sequential circuits : Static and Dynamic circuits.	Chalk & Talk
12.	Week 12 23-27 March 2020 (1+2 Contact hours)	**ASSESSMENT 2** True single-phase clocked registers – clocking schemes.	Chalk & Talk
13.	Week 13 30 Mar-3 April 2020 (3 Contact hours)	ASIC – Types of ASICs – Design flow – Design Entry – Simulation – Synthesis.	PPT
14.	Week 14 6-10 April 2020 (2 Contact hours)	Floor planning – Placement - Routing	PPT
15.	Week 15 13-17 April 2020 (3 Contact hours)	Circuit extraction – Programmable ASICs	PPT
16.	Week 16 20-24 April 2020 (3 Contact hours)	*Compensation Assessment (CPA)*	
17.	Week 17/18/19 27 April-13 May 2020	*End Semester Examination* (Final *Assessment*)	

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week	Duration	% Weightage
1	I[st] Class Test	Week 7 17-21 Feb 2020	60 minutes	20

2	II[nd] Class Test	Week 12 23-27 March 2020	60 minutes	20
3	Assignments	Throughout semester		10
CPA	Compensation Assessment	Week 16 20-24 April 2020	60 minutes	20
4	Final Assessment	Week 17/18/19 27 April-13 May 2020	180 minutes	50

Books and References

Text Books:

1. Neil Weste, David Harris, 'CMOS VLSI Design: A Circuits and Systems Perspective', Addison-Wesley, 4th Edition, 2010.
2. Debaprasad Das, 'VLSI Design', Oxford University Press, 2010.
3. Ken Martin, 'Digital Integrated Circuits', Oxford University Press, 1999.
4. Peter Van, 'Microchip Fabrication', Mc-Graw Hill Professional, 6th Edition, 2014.

Reference Books:

1. M. J. S. Smith, 'Application Specific Integrated Circuits', Addison Wesley, 1997.
2. Uyemura, 'Introduction to VLSI Circuits and Systems', Wiley, 1st Edition, 2012.

COURSE EXIT SURVEY

- Feedback from the students during class committee meetings
- Anonymous feedback through questionnaire (Mid of the semester & End of the semester)
- End semester feedback on course outcomes

COURSE POLICY (including compensation assessment to be specified)

1. Attending all the assessments mandatory for every student
2. One compensation assessment will be conducted for those students who are being physically absent for the assessment 1 and/or 2, only for the valid reason.
3. At any case CPA will not be considered as an improvement test.
4. Absolute/Relative grading will be adopted for the course.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION, IF ANY

FOR APPROVAL

Course Faculty _____ **CC- Chairperson** _____ **HOD** _____

Guidelines

a) The number of assessments for any theory course shall range from 4 to 6.

b) Every theory course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.

d) The passing minimum shall be as per the regulations.

B.Tech. Admitted in				P.G.
2018	2017	2016	2015	
35% or (Class average/2) whichever is greater.		(Peak/3) or (Class Average/2) whichever is lower		40%

e) Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

f) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

g) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.