DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	**VLSI DESIGN**		
Course Code	**EEPC24**	**No. of Credits**	**03**
Course Code of Pre-requisite subject(s)	**--**		
Session	**January 2019**	**Section (if, applicable)**	**B**
Name of Faculty	**V.Thenmozhi**	**ECE Department**	**B.Tech (EEE)**
Email	**mozhi@nitt.edu**	**Telephone No.**	**9677940537**
Name of Course Coordinator	**-**		
E-mail	**--**	**Telephone No.**	**--**
Course Type	**PC**		

Syllabus (approved in BoS)

- MOS characteristics: NMOS characteristics, inverter action – CMOS characteristics, inverter action -models and second order effects of MOS transistors – Current equation – MOSFET Capacitances -MOS as Switch, Diode/ resistor – current source and sink – Current mirror.
- CMOS Fabrication – n-well, p-well, twin-tub processes – fabrication steps – crystal growth –photolithography – oxidation – diffusion – Ion implantation – etching – metallization.
- CMOS Logic Circuits: Implementation of logic circuits using nMOS and CMOS, Pass transistor and transmission gates – Implementation of combinational circuits – parity generator – magnitude comparator – stick diagram – layout design.
- Memory design – SRAM cell – 6T SRAM – DRAM – 1T, 3T, 4T cells, CMOS Sequential circuits: Staticand Dynamic circuits – True Single-phase clocked registers – Clocking schemes.
- ASIC - Types of ASICs - Design flow – Design Entry – Simulation – Synthesis – Floor planning –Placement – Routing - Circuit extraction – Programmable ASICs.

COURSE OBJECTIVES

To enrich the student with the concepts of VLSI devices and its fabrication and also to develop Different electronic circuits.

COURSE OUTCOMES (CO)

1. To understand the insights of the MOS devices and its characteristics.
2. To appreciate the different VLSI process technologies.
3. To design the CMOS combinational logic circuits and its layout.
4. To develop the sequential circuits and clocking schemes.
5. To realize the Design flow of application-specific Integrated circuit.

COURSE OUTCOMES	**Aligned Programme Outcomes (PO)**
1. To understand the insights of the MOS devices and its characteristics.	**PO2, PO 7, PO 9, PO 13**
2. To appreciate the different VLSI process technologies.	**PO 3, PO 8**
3. To design the CMOS combinational logic circuits and its layout.	**PO 2, PO 3, PO 8, PO 14**
4. To develop the sequential circuits and clocking schemes.	**PO 2, PO 3, PO 8, PO 10, PO 14**
5. To realize the Design flow of application-specific Integrated circuit.	**PO 4, PO 8**

COURSE PLAN – PART II

COURSE OVERVIEW

This course provides the knowledge about NMOS, and CMOS technologies. Students will be able to learn about Programmable memory design and able to different ASIC & FPGA. They can acquire knowledge of fabrication of IC's and types of CMOS logic circuits.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No	Week/Contact Hours	Topic	Mode of Delivery
1.	Week 1 (**3 Contact Hours)**	Introduction to VLSI –MOS operation with current equation for all regions, mos capacitor for all regions, mos invertor action, pull up realization with comparisons.	**Lecture C&T**
2.	Week 2 **(3 Contact Hours)**	Dc transfer characteristics of mos invertor, Noise margin, output voltage realization for invertor for dc characteristics, small signal analysis of mosfet. Mos switch / resistor / diode and second order effect of mosfet, current source and sink, current mirror.	**Lecture C&T**

3.	Week 3 **(3 Contact Hours)**	MOS transistor analysis with solved problems. CMOS logic circuits implementation for parity generator and magnitude comparator –static CMOS (for all possible combinational circuits), Pass transistor logic realization, design rules, merits, demerits and solution	**Lecture** **C&T**
	ASSESSMENT I - 5 Marks		
4.	Week 4 **(3 Contact Hours)**	Implementation using complementary PTL, transmission gate, and pseudo NMOS logic, dynamic CMOS logic(with flip-flop design), dynamo CMOS logic, NORA CMOS logic.	**Lecture** **C&T/ PPT or any suitable mode**
5.	Week 5	**ASSESSMENT II - 20 Marks**	**Descriptive / Numerical (Written)**
6.	Week 6 **(3 Contact Hours)**	ZIPPER CMOS logic, TSPC logic, adiabatic logic, Implementation of sequential circuits using all design methods.	**Lecture** **C&T**
7.	Week 7 **(3 Contact Hours)**	Stick diagram – layout design for logic circuits, Memory design – SRAM cell – 6T SRAM – DRAM – 1T, 3T, 4T cells.	**Lecture** **C&T**
8.	Week 8 **(3 Contact Hours)**	CMOS Sequential circuits: Static and Dynamic circuits – True Single-phase clocked registers	**Lecture** **C&T/ PPT or any suitable mode**
	ASSESSMENT III - 5 Marks		
9.	Week 9 **(3 Contact Hours)**	Clocking schemes. CMOS Fabrication – n-well, p-well, twin-tub processes	**Lecture** **C&T/ PPT or any suitable mode**
10.	Week 10	**ASSESSMENT VI - 20 Marks**	**Descriptive / Numerical (Written)**
11.	Week 11 **(3 Contact Hours)**	Fabrication steps – crystal growth – Photolithography – oxidation – diffusion– Ion implantation – etching – metallization.	**Lecture** **C&T/ PPT or any suitable mode**
12.	Week 12 **(3 Contact Hours)**	ASIC - Types of ASICs - Design flow – Design Entry – Simulation	**Lecture** **C&T/ PPT or any suitable mode**

13.	Week 13 **(3 Contact Hours)**	Detail explanation about Synthesis – Floor planning –Placement – Routing - Circuit extraction.	**C&T/ PPT or any suitable mode**
14.	Week 14 **(3 Contact Hours)**	Programmable ASICs. Comparison with FPGA.	**Lecture** **C&T/ PPT or any suitable mode**

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment I	1st week Feb		5
2	Assessment II (CT I)	3rd Week Feb	60 Minutes	20
3	Assessment III	2nd Week of March		5
4	Assessment IV (CT II)	4th Week of March	60 Minutes	20
5	Assessment V (CPA)	1st Week of April	60 Minutes	20
6	End Assessment	4th Week of April	180 Minutes	50

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

CORRESPONDENCE

1. All the students are advised to check their NITT WEBMAIL/group mail/suggested by the course faculty, class representative regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through them only.
2. Queries (if required) to the course teacher shall only be emailed to the email id specified by the teacher.

ATTENDANCE

3. Attendance will be taken by the faculty in all the contact hours. Every student should try to be present in the class during these contact hours.
4. Those students who missed any of the continuous assessments (CAs) due to genuine reasons can appear for retest. The scores in the retest will be taken into account for computing marks for CA.

ASSESSMENT

5. Attending all the assessments are MANDATORY for every student.
6. Every student is expected to score minimum 40% of the maximum mark of the class in the

total assessment (1, 2, 3, 4 and 6) to pass the course. Otherwise the student would be declared fail and 'F' grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any Assessments are considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL INFORMATION

FOR APPROVAL

Course Faculty 4/2/19 CC-Chairperson 4/2/19 **HOD**