NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE PLAN – PART I			
Name of the programme and specialization	**B.Tech. (CSE)**		
Course Title	**Computer Organization**		
Course Code	**CSMI12**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**NIL**		
Session	**January 2019**	**Section (if, applicable)**	**A & B**
Name of Faculty	**C. Nandhini**	**Department**	**CSE**
Official Email	nandhinic@nitt.edu	**Telephone No.**	
Name of Course Coordinator(s) (if, applicable)			
Official E-mail		**Telephone No.**	
Course Type (please tick appropriately)	☐ **Core course**	☑ **Elective course**	

Syllabus (approved in Senate)

Unit I:
Introduction, Technologies for building Processors and Memory, Performance, The Power Wall, Operations of the Computer Hardware, Operands Signed and Unsigned numbers, Representing Instructions, Logical Operations, Instructions for Making Decisions.

Unit – II:
MIPS Addressing for 32-Bit Immediate and Addresses, Parallelism and Instructions: Synchronization, Translating and Starting a Program, Addition and Subtraction, Multiplication, Division, Floating Point, Parallelism and Computer Arithmetic: Subword Parallelism, Streaming SIMD Extensions.

Unit – III:
Logic Design Conventions, Building a Datapath, A Simple Implementation Scheme, overview of Pipelining, Pipelined Datapath, Data Hazards: Forwarding versus Stalling, Control Hazards, Exceptions, Parallelism via Instructions.

Unit – IV:
Memory Technologies, Basics of Caches, Measuring and Improving Cache Performance, dependable memory hierarchy, Virtual Machines, Virtual Memory, Using FSM to Control a Simple Cache, Parallelism and Memory Hierarchy: Redundant Arrays of Inexpensive Disks.

Unit – V:

Disk Storage and Dependability, Parallelism and Memory Hierarchy: RAID levels, Performance of storage systems, Introduction to multi threading clusters, message passing multiprocessors.

Text Books

1. David A. Patterson and John L. Hennessey, "Computer organization and design, The Hardware/Software interface", Morgan Kauffman / Elsevier, Fifth edition, 2014.

2. Smruti Ranjan Sarangi, "Computer Organization and Architecture", McGraw Hill Education, 2015.

COURSE OBJECTIVES

- To understand the basic hardware and software issues of computer organization
- To understand the representation of data at machine level
- To understand how computations are performed at machine level

MAPPING OF COs with Pos

Course Outcomes	Programme Outcomes (PO) (Enter Numbers only)
1. Ability to analyze the abstraction of various components of a computer	**1, 3**
2. Ability to analyze the hardware and software issues and the interfacing	**1, 6, 8**
3. Ability to design and develop components of ARM processor	**1, 2, 5, 6**

COURSE PLAN – PART II

COURSE OVERVIEW

This course will introduce students to the fundamental concepts underlying modern computer organization. Main objective of the course is to familiarize students about hardware design including logic design, basic structure and behavior

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	1/1	Introduction, Technologies for building Processors and Memory	Chalk and Board
2	1/2	Operations of the Computer Hardware, Operands	Chalk and Board
3	1/3	Signed and Unsigned numbers	Chalk and Board
4	2/1	Representing Instructions	Chalk and Board
5	2/2	Logical Operations,	Chalk and Board

6	2/3	Instructions for Making Decisions.	Chalk and Board
7	3/1	Performance, The Power Wall	Chalk and Board
8	3/2	MIPS Addressing for 32-Bit Immediates and Addresses	Chalk and Board
9	3/3	Parallelism and Instructions: Synchronization	Chalk and Board
10	4/1	Translating and Starting a Program	Chalk and Board
11	4/2	Addition and Subtraction	Chalk and Board
12	4/3	Multiplication	Chalk and Board
13	5/1	Division	Chalk and Board
14	5/2	Floating Point	Chalk and Board
15	5/3	Parallelism and Computer Arithmetic	Chalk and Board
16	6/1	Subword Parallelism.	Chalk and Board
17	6/2	Streaming SIMD Extensions	Chalk and Board
18	6/3	Logic Design Conventions	Chalk and Board
19	7/1	Building a Datapath	Chalk and Board
20	7/2	A Simple Implementation Scheme	Chalk and Board
21	7/3	An Overview of Pipelining	Chalk and Board
22	8/1	Pipelined Datapath and Control	Chalk and Board
23	8/2	Data Hazards: Forwarding versus Stalling	Chalk and Board
24	8/3	Control Hazards, Exceptions	Chalk and Board
25	9/1	Parallelism via Instructions	Chalk and Board
26	9/2	Memory Technologies, The Basics of Caches	Chalk and Board
27	9/3	Measuring and Improving Cache Performance	Chalk and Board
28	10/1	Dependable Memory Hierarchy	Chalk and Board
29	10/2	Virtual Machines	Chalk and Board
30	10/3	Virtual Memory	Chalk and Board
31	11/1	Using a FSM to Control a Simple Cache	Chalk and Board
32	11/2	Parallelism and Memory Hierarchy: Redundant Arrays of Inexpensive Disks	Chalk and Board
33	11/3	Disk Storage and Dependability,	Chalk and Board
34	12/1	RAID levels	Chalk and Board
35	12/2	Performance of storage systems	Chalk and Board
36	12/3	Introduction to multi threading clusters	Chalk and Board
37	13/1	Message passing multiprocessors.	Chalk and Board

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Cycle Test-1	3rd week of Feb	1 hour	20
2	Assignment	2nd week of Mar	1 week	10
3	Cycle Test-2	1st week of Apr	1 hour	20
CPA	Compensation Assessment*	2nd week of Apr	1 hour	20
4	Final Assessment *	2nd week of May	3 hours	50

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Students through their class representative may give their feedback at any time to the course faculty which will be duly addressed. Students may also give their feedback during class committee meeting. Feedback questionnaire from students – from MIS at the end of the semester.

COURSE POLICY (including compensation assessment to be specified)

Students should not absent for assessments. If the reason for absence is genuine, the student can appear for compensation assessment. The medical certificate/on duty certificate should be submitted within one week after rejoining.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and

award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

- The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION, IF ANY

FOR APPROVAL

Course Faculty _____ **CC- Chairperson** _____ **HOD** _____ 29/1/19

Guidelines

a) The number of assessments for any theory course shall range from 4 to 6.

b) Every theory course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.

d) The passing minimum shall be as per the regulations.

B.Tech. Admitted in				P.G.
2018	2017	2016	2015	
35% or (Class average/2) whichever is greater.		(Peak/3) or (Class Average/2) whichever is lower		40%

e) Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

f) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

g) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.