DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I				
Course Title	**Micro-computing and VLSI Design Lab**			
Course Code	**EE LR 16**	**No. of Credits**	**03**	
Course Code of Pre-requisite subject(s)	**EEPC22, EEPC24**			
Session	**~~July/~~ Jan. 2018**	**Section**	**B**	
Name of Faculty	**Dr. S. Moorthi**	**Department**	**EEE**	
Email	**mcvlsi.moorthi@gmail.com**	**Telephone o.**		
Name of Course Coordinator(s)	-			
E-mail		**Telephone No.**		
Course Type	√ **Core course**	☐ **Elective course**		

Syllabus (approved in BoS)

List of Experiments

- Arithmetic operations (8/ 16 bit) using 8085
- Waveform generation using 8085
- Interfacing with 8085 (ADC, DAC)
- Arithmetic operations (16 bit) using 8051
- Firing pulse generation using 8051
- Interfacing with 8051 (Stepper motor/ DC Motor control)
- VHDL programming for PWM pulse generation
- Design and Simulation of Sequence detector circuit using Verilog HDL
- Design and FPGA implementation of 4-bit multiplier unit
- Layout and physical design of a Mod-N counter unit

Mini–Project

COURSE OBJECTIVES

To train the students to use micro-processor, micro-controller and FPGA for computational and logical applications. Also, this course prepares the students to provide solutions to real-time problems.

COURSE OUTCOMES (CO):

Upon completion of the course, the student will be able to	**Aligned Programme Outcomes (PO)**
1. Accomplish arithmetic and logical operations with micro-processors, micro-controllers and FPGA.	**PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PO12, PO13, PO14.**
2. Generate firing pulses for various control applications related to electrical machines and power electronics.	
3. Illustrate various interfacing techniques related to real-time applications using microprocessors and micro-controllers.	
4. Analyze and document the experiments carried out.	
5. Design and implement control circuitry using micro-processors and micro-controllers for any engineering and real world problems.	

COURSE PLAN – PART II			
COURSE OVERVIEW			
This is a course to provide exposure and hands-on training to the students on practical implementations of processors and controllers in addition to the programmable devices like FPGAs.			
COURSE TEACHING AND LEARNING ACTIVITIES			
S.No.	**Week/Contact Hours**	**Topic**	**Mode of Delivery**
1	**Week 1**	Introduction and Lab visit to know the equipment used in lab.	C&T, Practical
2	**Week 2**	Arithmetic programming using 8085	C&T, Practical
3	**Week 3**	Programming to play with numbers using 8085	C&T, Practical
4	**Week 4**	Waveform generation using 8085	C&T, Practical
5	**Week 5**	Peripheral interfacing with 8085	C&T, Practical
6	**Week 6**	Arithmetic programming using 8051	C&T, Practical
7	**Week 7**	Programming to play with numbers using 8051	C&T, Practical
8	**Week 8**	Waveform generation using 8051	C&T, Practical
9	**Week 9**	Peripheral interfacing with 8051	C&T, Practical
10	**Week 10**	VHDL programming and simulation for a sequence detector	C&T, Practical
11	**Week 11**	FPGA implementation of the sequence detector	C&T, Practical
12	**Week 12**	Mini project evaluation	--

COURSE ASSESSMENT METHODS (shall range from 4 to 6)				
S.No.	**Mode of Assessment**	**Week/Date**	**Duration**	**% Weightage**
1	Continuous Session Assessment (CSA)* (Program, Execution & Result)	Every week	--	40
2	Report	Every week	--	10
CPA	Compensation Assessment*	--	--	--
3	Final Assessment 1 – Viva Test	Week 10	One hour	25
4	Final Assessment 2 – Mini project Evaluation	At the end of the semester (Week 12)	--	25

* **If an experiment of a particular session (Week 1) is incomplete, it can be carried over to the immediate subsequent week (Week 2) only; which will serve as the time for re-assessing the experiment. However, the maximum marks that will be awarded is as given below:**

S.No.	Status	Program	Execution	Result
1.	Program verfication, Execution and Results – all done in **Week 1**	25	10	05
2.	Program verification done – **Week 1** Execution and Results – **Week 2**	25	05	05
3.	Program verfication, Execution and Results – all done in **Week 2**	05	05	05
4.	Program verification alone done in **Week 2.** Execution and results not obtained in **Week 2** also.	05	00	00

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings

Anonymous feedback through questionnaire (Mid of the semester & End of the semester)

End semester feedback on Course Outcomes

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

1. **All the students are advised to check their NITT WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail only.**
2. **Queries (if required) to the course teacher shall only be emailed to mcvlsi.moorthi@gmail.com**

ATTENDANCE

1. Attendance will be taken by the faculty in all the lab sessions.
2. Attendance of ALL STUDENTS is EXPECTED for the lab sessions mentioned. Every student should maintain minimum 75 % attendance in these lab sessions to attend the final assessments (Viva Test and mini-project evaluation).
3. Students not having sufficient attendance (75%) at the end of the semester will have to RE-DO the course.

COMPENSATION ASSESSMENT

1. If a student is absent for a lab session for a genuine reason, it will be considered and compensation will be given in the next immediate session itself. However, the honesty and genuineness of the reason will be analysed and decided by the course faculty. Also, a new question will be given for the student.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any assessments is considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.

   Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL INFORMATION
NIL
FOR APPROVAL

Course Faculty _____ 12/1/2018 CC-Chairperson _____ HOD _____ 15/01/2018