NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE OUTLINE TEMPLATE										
Course	e Title	Digital Electronics								
Course	e Code	EEPC	:15		No. of Credits		03			
Depart	ment	EEE			Faculty					
Pre-rec	quisites	Esse	Essentials of Electron Devices(EEPC10)							
Course	e Code									
Coordi	; inator(s)									
(if. app	licable)									
Other (Course		Telephone No. 0431-2503267							
Teache	er(s)/Tutor(s)									
Course	е Туре	\checkmark	Core c	ourse	Elective	course				
COUR	SE OVERVIEW									
This is further	a basic course into the differe	to tead nt logi	ch Digita c circuits	I fundamenta ike combir	als which s national an	starts with d sequent	number syster ial in detail.	ns and move		
COUR	SE OBJECTIVES	3				•				
This su	ubject exposes t	the stu	dents to	digital funda	amentals					
COUR	SE OUTCOMES	(CO)								
On completion of the course the students would be able to: Aligned Programme Outcomes (PO)								itcomes (PO)		
1. Interpret, convert and represent different number PO1, P					PO1, PO)2, PO3, PO6, PO8, PO9,				
2. Mai	nipulate and exa	amine l	Boolean	algebra, logi	ic	F010, F0	513.			
operat	ions, Boolean fu	unctior	is and th	eir simplifica	ation.					
3. Desi	3. Design and analyze combinational and sequential logic									
circuit										
S No	URSE TEACHING AND LEARNING ACTIVITIES						Mode of			
5.140.	, ve	VVEEK			Topic			Delivery		
1.	1 (two hours)			Review of r	number systems,			C&T		
2.	1 (one hour), 2	(one h	nour)	Binary codes – BCD and computations			C&T, PPTs			
	, <i>j</i> ,	•	error detection and correction codes. Diaital				· -			
3.	2 (two hours),3	(two hours) Logic families.RTL,DTL,TTL,ECL and MOSL				C&T				
4.	3 (one hour)	e hour)			Objective Test					
5.	3(One hour),			Combinational logic - representation of logic				C&T		
4 (three hours) functions – SOP and POS forms K-map					s K-map					
6	5 (two bours)			representat	on and imr	Imization	using K maps	C&T DDT		
0.	5 (100 110015)	simplification and implementation of C&I, PPI						GA 1, FF1		
			demultiplexers							
7.	5 (one hour),	one hour),			code converters, adders, subtractors			PPT, C&T		
	6 (two hours)	(two hours)			(Hands-on Test – 1)					
8.	6 (one hour)	Ubjective cum D			Im Design	1 Design Test				
9.	/ (two hours)	Sequential logic- SR, JK, D and T flip flops – C&T, PPT					C&I, PPT			
				ievei trigge	ing and ed	ige trigge	inig			

B (three hours), 9 (three hours) counters - asynchronous and synchronous type - Modulo counters (Flip-class 11. 10 (two hours) Shift registers - Ring counters. C&T,PPT 12. 10 (one hour), 11 (one hour), Synchronous Sequential Logic circuits-state C&T,PPT C&T,PPT 13. 11 (one hour) Analogy Model Evaluation - 14. 11 (one hour) Analogy Model Evaluation - 15. 12 (three hours) Design of counters-analysis of synchronous sequential logic circuits- state assignment. C&T,PPT 16. 13 (three hours) Asynchronous sequential logic circuits. Transition table, flow table - race conditions asynchronous sequential logic circuits. C&T,PPT 17. 14 (two hours) Introduction to design - implication table - hazards. C&T,PPT 18. 14 (one hour), 15 (three hours) Programmable logic array and devices. C&T,PPT 19. 16 (one hour) Compensation Assessment (CPA) COURSE ASSESMENT METHODS C&T,PPT 2. Hands-on Test - 1 6 One hour 15 2. Hands-on Test - 2 8 One hour 15 3. <th>10.</th> <th>7 (one hour),</th> <th>Hands-on T</th> <th>C&T, PPT</th>	10.	7 (one hour),	Hands-on T	C&T, PPT					
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4. Hands-on Test - 2 8 One hour 15 5. Analogy Model (Group - 2 members) 11 One hour 10 - Compensation Assessment (CPA) 16 One hour 15* 6. Final Written Exam End of semester Two hours 30 * Conditions for Compensation Assessment (CPA) may be referred in Assessment section (explained below). ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc Text Books: 1. Morris Mano.M, 'Digital logic and computer design', Prentice Hall of India, 3rd Edition, 2005. 2. Donald D. Givone, 'Digital Principles and Design', Tata McGraw Hill, 1st Edition, 2002. Reference Books: 1. Tocci R.J.,Neal S. Widmer, 'Digital Systems: Principles and Applications', Pearson Education Asia, 2014. 2. Donald P Leach, Albert Paul Malvino, Goutam Sha, 'Digital Principles and Applications', The McGraw Hill, 7th edition, 2010. COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also) Feedback from the students during class committee meetings Anonymous feedback through questionnaire End semester feedback on Course Outcomes	3.	Objective cum Design test		6	One hour	15			
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End semester feedback on Course Outcomes	Anonymous feedback through questionnaire								
	End semester feedback on Course Outcomes								

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

CORRESPONDENCE

- 1. All the students are advised to check their WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail only.
- 2. Queries (if required) to the course teacher shall only be emailed to smoorthi.digital@gmail.com

ASSESSMENT

- 1. Attending all the assessments are MANDATORY for every student.
- 2. If any student is not able to attend any of the continuous assessments CAs: 1 and 3 (refer SI. Nos. in course assessment methods) due to genuine reason, student is permitted to attend the compensation assessment (CPA) with % weightage equal to maximum of the CAs. However, maximum of the % weightage among the assessments for which the student was absent will be considered for computing marks for CA.
- 3. At any case, CPA will not be considered as an improvement test.
- 4. The minimum marks for passing this course and grading pattern will adhere to the regulations of the Institute.

ATTENDANCE

- 1. Attendance will be taken by the faculty in all the contact hours.
- 2. Attendance of ALL STUDENTS is EXPECTED for the physical contact hours mentioned. Every student should maintain minimum 75 % attendance in these contact hours to attend the Final Written Examination.
- 3. Any student, who fails to maintain 75% and secured more than 50% marks in the assessments conducted (SI. No. 1 to 5 in the course assessment methods) will be permitted to attend the final written exam.
- 4. Students not having sufficient attendance (75%) at the end of the semester and also fail to score the required marks (50%) in assessments (as mentioned in Point: 3, above) will have to RE-DO the course.

ACADEMIC HONESTY & PLAGIARISM

- 1. All the students are expected to do their own work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during an examination is considered dishonest.
- 2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
- 3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty. Any evidence of such academic dishonesty will result in the loss of all marks on that assignment or examination. Additionally, the names of those students so penalized will be reported to the Office of Dean (Students), Office of Dean (Academic) and Training & Placement Cell for the records.
- 4. Students who honestly produce original and OUTSTANDING WORK will be REWARDED with additional marks.

ADDITIONAL COURSE INFORMATION								
The Course Coordinator is available for consultation at times that is displayed on the coordinator's office notice board.								
Queries may also be emailed to the Course	Coordinator directly at smoo	rthi.digital@gmail.com						
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