DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE OUTLINE TEMPLATE			
Course Title	**CIRCUIT THEORY III Sem. EEE – B Section**		
Course Code	**EEPC11**	**No. of Credits**	**04**
Department	**EEE**	**Faculty**	**N. Kumaresan**
Pre-requisites Course Code	**MAIR21**		
Course Coordinator(s)	**---**		
Other Course Teacher(s) / Tutor(s) E-mail	**---**	**Telephone No.**	**0431-2503257**
Course Type	√ **Core course** ☐ **Elective course**		

COURSE OVERVIEW

An electric circuit is a mathematical model that approximates the behaviour of an actual electrical system. Circuit analysis has long been a traditional introduction to the art of problem solving from an engineering perspective, even for those whose interests lie outside electrical engineering. There are many reasons for this, but one of the best is that in today's world it's extremely unlikely for any engineer to encounter a system that does not in some way include electrical circuitry. They are found in homes, schools, workplaces and transportation vehicles everywhere.

Since most engineering situations require a team effort at some stage, having a working knowledge of circuit analysis therefore helps to provide everyone on a project with the background needed for effective communication. The models, the mathematical technique, and the language of circuit theory will form the intellectual framework for our engineering endeavours. Hence, this course on Circuit Theory is about developing basic problem-solving skills as they apply to situations an engineer is likely to encounter.

The focus of this course is on linear circuit analysis. Linear problems are inherently more easily solved than their nonlinear counterparts. For this reason, we often seek reasonably accurate linear approximations (or models) to physical situations. Furthermore, the linear models are more easily manipulated and understood—making design a more straightforward process. When greater accuracy is required in practice, nonlinear models are employed, but with a considerable increase in solution complexity.

Linear circuit analysis can be separated into four broad categories: (1) dc analysis, where the energy sources do not change with time; (2) transient analysis, where things often change quickly; (3) sinusoidal analysis, which applies to both ac power and signals; and (4) frequency response, which is the most general of the four categories, but typically assumes something is changing with time.

This course begin with the topic of resistive circuits to learn a number of very powerful engineering circuit analysis techniques, such as nodal analysis, mesh analysis, superposition, source transformation, Thévenin's theorem, Norton's theorem, and several methods for simplifying networks of components connected in series or parallel. Then, the analysis of the circuits with ac source and related components are introduced. To study circuits which are suddenly energized or de-energized, transient analysis of simple RL, RL and RLC are also included in this course.

COURSE OBJECTIVES

To provide the key concepts and tools in a logical sequence to analyze and understand electrical and electronic circuits.

COURSE OUTCOMES (COs)

Upon completion of the course, the students will be able to

1. Understand the technical representation of common electrical systems.
2. Analyze and compute the time domain behavior of linear (AC and DC) electric circuits with single or multiple power sources.
3. Compute the performance of AC Networks (1-port) which may be 1-phase or 3-phase using phasor analysis.
4. Understand the flow of real and reactive power components in AC systems.
5. Analyze simple electro-magnetic circuits.

Aligned Programme Outcomes (POs)

COs / POs		Course outcomes(COs)				
		1	2	3	4	5
Programme Outcomes (POs)	1	H	H	H	H	H
	2	L	M	M	M	M
	3	NA	H	H	H	H
	4	NA	M	M	HL	M
	5	L	M	H	H	M
	6	NA	NA	NA	NA	NA
	7	L	M	M	M	L
	8	L	H	H	H	M
	9	NA	M	M	M	M
	10	L	M	H	H	H
	11	NA	NA	NA	NA	NA
	12	L	M	H	H	H
	13	H	H	H	H	H
	14	L	M	M	M	M

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
1.	17 – 21 July '17 **(4 Contact Hours)**	Discussion on course plan DC circuits – series and parallel circuits – loop and nodal analysis	Lecture / Tutorial C & T using Document viewer
2.	24 – 28 July '17 **(4 Contact Hours)**	DC circuits –contd.. AC circuits – Impedance, phasor diagram, real and reactive power	
3.	31 July – 4 August '17 **(4 Contact Hours)** **04.08.2017 : 50 minutes (2.20 pm – 3.10 pm)**	AC circuits : Loop and nodal analysis **(Assessment-3 : Problem solving / numerical examples from Unit I – 5 marks)**	
4.	7 – 11 August '17 **(4 Contact Hours)**	Source transformation, network theorems, equivalent circuits, star-delta transformation	
5.	14 – 18 August '17 **(3 Contact Hours)**		
6.	21 – 24 August '17 **(3 Contact Hours)** **21.08.2017 : 50 minutes (2.20 pm – 3.10 pm)**	Resonance in series and parallel circuits **(Assessment-3 : Problem solving / numerical examples from Unit II – 5 marks)**	
7.	28 August '17 to 1 September '17 **(4 Contact Hours)**	Self and mutual inductances, coefficient of coupling – dot convention – analysis of coupled circuits **(Assessment - 1) Written test (Unit I and II)**	
8.	4 – 8 September '17 **(4 Contact Hours)** **21.08.2017 : 50 minutes (2.20 pm – 3.10 pm)**	Analysis of coupled circuits – contd.. **(Assessment-3 : Problem solving / numerical examples from Unit III – 5 marks)**	

S.No.	Week	Topic	
9.	11 – 15 September '17 **(4 Contact Hours)**	Introduction to offline simulation	Lecture Hands-on experience
10.	18 – 22 September '17 **(2 Contact Hours)**	Simulation of circuit transients – using c/c++ programming	
11.	25 – 29 September '17 **(2 Contact Hours)**	**(Assessment-3 : Offline simulation of circuits : 5 marks)**	
12.	3 – 6 October '17 **(3 Contact Hours)**	**Assessment-3 contd..** **(Assessment - 2) Written test (Unit III and V)**	
13.	9 – 13 October '17 **(4 Contact Hours)**	Three-phase star and delta connected circuits with balanced and unbalanced loads – power measurements – power factor calculations	Lecture / Tutorial C & T using Document viewer
14.	16 – 20 October '17 **(2 Contact Hours)**		
15.	23-27 October '17 **(4 Contact Hours)**		
16.	30.10.17 to 3.11.17 **(4 Contact Hours)**	Review and doubt clearing classes	
17.	6-10 November '17 **(1 Contact Hour)**	CPA	
18.	13-11-17 to 22-11-17	**ASSESSMENT – 4** (written test) Date of examination will be intimated later	

C & T : Chalk and Talk and PPT : Power Point

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment-1 (First 2 Units) : **(Written test)**	28 August '17 to 1 September '17	60 Minutes	20
2	Assessment-2 (3rd and 5th Units) : **(Written test)**	3 – 6 October '17	60 Minutes	20
3	Assessment-3 Assignment (4 Nos. each for 5 marks)	During the regular class hours – details will be informed later		20
CPA	Compensation Assessment **(Written test)**	6-10 November '17	60 Minutes	20
5	Assessment-4 (All units) : **(Written test)**	13.11.17 to 22.11.17	120 Minutes	40

Note:

1. Exact date and time for the assessments (1,2, 4 and CPA) will be informed later.
2. Attending all the assessments (i.e., Assessment 1 to 4) are MANDATORY for every student.
3. If any student is not able to attend Assessment-1 / Assessment-2 due to genuine reason, he/she is permitted to attend the Compensation Assessment (CPA) with 20% weightage (20 marks).
4. At any case, CPA will not be considered as an improvement test.

Grading the students

1. Grading will be based on the clusters (range) of the total marks (all the assessments i.e., Assessment 1 to 4, put together for each student) scored. For grading, Gap theory or Normalized curve method will be used to decide the clusters (range) of the total marks.

2. The passing minimum shall be class mean by two or maximum by three, whichever is lower. Hence, every student is expected to score the minimum mark to pass the course. Otherwise the student would be declared fail and 'F' grade will be awarded.

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

1. *Hayt, W. H, Kemmerly J. E. & Durbin, 'Engineering Circuit Analysis', McGraw Hill Publications, 8th Edition, 2013.*
2. *James W. Nilsson and Susan A. Riedel, 'Electric Circuits', Pearson Education Publications, 9th Edition, 2011.*
3. *Charles K. Alexander, Matthew N.O.Sadiku, 'Fundamentals of Electric Circuits', McGraw-Hill Publications, 5th Edition, 2013.*
4. *Joseph. A. Edminister, 'Electric Circuits - Schaum's Outline Series', McGraw-Hill Publications, 6th Edition, 2003.*
5. *Robins & Miller, 'Circuit Analysis Theory and Practice', Delmar Publishers, 5th Edition, 2012.*

Following NPTEL course materials will form the additional references :

1. Basic Electrical Circuits by Dr Nagendra Krishnapura, Department of Electrical Engineering, IIT Madras. Web-site: http://nptel.ac.in/courses/117106108/#

2. Circuit theory by Prof. S.C. Dutta Roy, IIT Delhi. Web-site : http://nptel.ac.in/courses/108102042/#

COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

CORRESPONDENCE

1. All the students are advised to check their NITT WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail.
2. Queries (if required) may be emailed to me / contact me during 10.30 am to 11.30 am on Monday and Wednesday with prior intimation for any clarifications.

ATTENDANCE

1. Attendance will be taken by the faculty in all the contact hours. Every student should maintain minimum 75 % physical attendance in these contact hours to attend the Assessment-4 i.e., last assessment.

2. Any student, who fails to maintain 75% attendance, however, having score more than 50 % marks (i.e., more than 30 marks) in first three assessments will be eligible for attending the last assessment (Assessment-4).

3. Students having less than 75% attendance at the end of the semester and also having the score less than 50 % marks (i.e., less than 30 marks) in first three assessments will have to REDO the course and hence they are not eligible for attending the last assessment (Assessment-4). 'V' Grade will be awarded for such students.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any assessments is considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD for necessary action.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL COURSE INFORMATION

FOR APPROVAL

Course Faculty	CC-Chairperson	HoD
		17/7/17