NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE OUTLINE TEMPLATE			
Course Title	Digital Electronics		
Course Code	EEPC15	No. of Credits	03
Department	EEE (2nd year A section)	Faculty	Mrs. S. Mageshwari
Pre-requisites Course Code	Essentials of Electron Devices(EEPC10)		
Course Coordinator(s) (if, applicable)	--		
Other Course Teacher(s)/Tutor(s)	--	Telephone No.	0431-2503260
Course Type	√ Core course	☐ Elective course	

COURSE OVERVIEW
This is a basic course to teach Digital fundamentals which starts with number systems and move further into the different logic circuits like combinational and sequential in detail.
COURSE OBJECTIVES
This subject exposes the students to digital fundamentals
COURSE OUTCOMES (CO)

On completion of the course the students would be able to:	Aligned Programme Outcomes (PO)
1. Interpret, convert and represent different number systems. 2. Manipulate and examine Boolean algebra, logic operations, Boolean functions and their simplification. 3. Design and analyze combinational and sequential logic circuits.	PO1, PO2, PO3, PO6, PO8, PO9, PO10, PO13.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
1.	1 (two hours)	Review of number systems,	C&T
2.	1 (one hour), 2 (one hour)	Binary codes – BCD and computations	C&T, PPTs
3.	2 (two hours),3(two hours)	error detection and correction codes. Digital Logic families:RTL,DTL,TTL,ECL and MOSL	C&T
4.	3 (one hour)	*Objective Test*	-
5.	3(One hour), 4 (three hours)	Combinational logic - representation of logic functions – SOP and POS forms K-map representations – minimization using K maps	C&T
6.	5 (two hours)	simplification and implementation of combinational logic – multiplexers and demultiplexers	C&T, PPT
7.	5 (one hour), 6 (two hours)	code converters, adders, subtractors *(Hands-on Test – 1)*	PPT, C&T
8.	6 (one hour)	*Objective cum Design Test*	-
9.	7 (two hours)	Sequential logic- SR, JK, D and T flip flops – level triggering and edge triggering	C&T, PPT

10.	7 (one hour), 8 (three hours), 9 (three hours)	*Hands-on Test - 2* counters – asynchronous and synchronous type – Modulo counters	C&T, PPT (Flip-class)
11.	10 (two hours)	Shift registers – Ring counters.	C&T,PPT
12.	10 (one hour), 11 (one hour).	Synchronous Sequential Logic circuits-state table and excitation tables-state diagrams	C&T,PPT (Flip-class)
13.	11 (one hour)	Moore and Mealy models	C&T,PPT
14.	11 (one hour)	*Analogy Model Evaluation*	-
15.	12 (three hours)	Design of counters-analysis of synchronous sequential logic circuits-state reduction and state assignment.	C&T, PPT (partly Flip-class)
16.	13 (three hours)	Asynchronous sequential logic circuits-Transition table, flow table – race conditions – circuits with latches, analysis of asynchronous sequential logic circuits.	C&T, PPT (partly Flip-class)
17.	14 (two hours)	Introduction to design – implication table – hazards.	C&T, PPT
18.	14 (one hour), 15 (three hours)	Programmable logic array and devices.	C&T, PPT
19.	16 (one hour)	*Compensation Assessment (CPA)*	

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Objective Test	3	30 minutes	15
2.	Hands-on Test – 1	6	One hour	15
3.	Objective cum Design test	6	One hour	15
4.	Hands-on Test – 2	8	One hour	15
5.	Analogy Model (Group – 2 members)	11	One hour	10
-	Compensation Assessment (CPA)	16	One hour	15*
6.	Final Written Exam	End of semester	Two hours	30

* Conditions for Compensation Assessment (CPA) may be referred in Assessment section (explained below).

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

Text Books:

1. Morris Mano.M, 'Digital logic and computer design', Prentice Hall of India, 3rd Edition, 2005.
2. Donald D. Givone, 'Digital Principles and Design', Tata McGraw Hill, 1st Edition, 2002.

Reference Books:

1. Tocci R.J.,Neal S. Widmer, 'Digital Systems: Principles and Applications', Pearson Education Asia, 2014.
2. Donald P Leach, Albert Paul Malvino, Goutam Sha, 'Digital Principles and Applications', The McGraw Hill, 7th edition, 2010.

COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire
End semester feedback on Course Outcomes

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

CORRESPONDENCE

1. All the students are advised to check their WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail only.

2. Queries (if required) to the course teacher shall only be emailed to digitalelectronics.eee@gmail.com

ASSESSMENT

1. Attending all the assessments are MANDATORY for every student.

2. If any student is not able to attend any of the continuous assessments CAs: 1 and 3 (refer Sl. Nos. in course assessment methods) due to genuine reason, student is permitted to attend the compensation assessment (CPA) with % weightage equal to maximum of the CAs. However, maximum of the % weightage among the assessments for which the student was absent will be considered for computing marks for CA.

3. At any case, CPA will not be considered as an improvement test.

4. The minimum marks for passing this course and grading pattern will adhere to the regulations of the Institute.

ATTENDANCE

1. Attendance will be taken by the faculty in all the contact hours.

2. Attendance of ALL STUDENTS is EXPECTED for the physical contact hours mentioned. Every student should maintain minimum 75 % attendance in these contact hours to attend the Final Written Examination.

3. Any student, who fails to maintain 75% and secured more than 50% marks in the assessments conducted (Sl. No. 1 to 5 in the course assessment methods) will be permitted to attend the final written exam.

4. Students not having sufficient attendance (75%) at the end of the semester and also fail to score the required marks (50%) in assessments (as mentioned in Point: 3, above) will have to RE-DO the course.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to do their own work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during an examination is considered dishonest.

2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.

3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty. Any evidence of such academic dishonesty will result in the loss of all marks on that assignment or examination. Additionally, the names of those students so penalized will be reported to the Office of Dean (Students), Office of Dean (Academic) and Training & Placement Cell for the records.

4. Students who honestly produce original and OUTSTANDING WORK will be REWARDED with additional marks.

ADDITIONAL COURSE INFORMATION

The Course Coordinator is available for consultation at times that is displayed on the coordinator's office notice board.

Queries may also be emailed to the Course Coordinator directly at digitalelectronics.eee@gmail.com

FOR SENATE'S CONSIDERATION

Course Faculty S. Meganathan CC-Chairperson _____ HOD _____ 10/07/2017