**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI**

| **COURSE PLAN – PART I** | | | |
|---|---|---|---|
| **Name of the programme and specialization** | **M.TECH, VLSI SYSTEM** | | |
| **Course Title** | **MODELING AND SYNTHESIS WITH VERILOG HDL** | | |
| **Course Code** | **EC662** | **No. of Credits** | **3** |
| **Course Code of Pre-requisite subject(s)** | **None** | | |
| **Session** | **July - 2021** | **Section (if, applicable)** | **-** |
| **Name of Faculty** | **Dr. Archana S** | **Department** | **Electronics and communication engineering** |
| **Email** | **sarchana@nitt.edu** | **Telephone No.** | **9447449202** |
| **Course Type** | **Elective course** | | |

**Syllabus (approved in BoS)**

Hardware modeling with the verilog HDL. Encapsulation, modeling primitives, different types of description.

Logic system, data types and operators for modeling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection.

Behavioral descriptions in verilogHDL.Synthesis of combinational logic.

HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.

Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives. Switch-level models in verilog. Design examples in verilog.

**COURSE OBJECTIVES**

- To design combinational, sequential circuits using Verilog HDL.
- To understand behavioral and RTL modeling of digital circuits
- To verify that a design meets its timing constraints, both manually and through the use of computer aided design tools
- To simulate, synthesize, and program their designs on a development board
- To verify and design the digital circuit by means of Computer Aided Engineering tools which involves in programming with the help of Verilog HDL.

| COURSE OUTCOMES (CO) | |
|---|---|
| **Course Outcomes** | **Aligned Programme Outcomes (PO)** |
| 1. Understand the basic concepts of verilog HDL | |
| 2. Model digital systems in verilog HDL at different levels of abstraction | |
| 3. Know the simulation techniques and test bench creation | |
| 4. Understand the design flow from simulation to synthesizable version | |
| 5. Get an idea of the process of synthesis and post-synthesis | |

**COURSE PLAN – PART II**

**COURSE OVERVIEW**

This course provides the knowledge about modelling of various digital circuits using Verilog HDL, their synthesis and post sysnthesis design flow. They can acquire knowledge realising behavioural and structural modelling of the circuits and also their simulation and test bench creation.

**COURSE TEACHING AND LEARNING ACTIVITIES**

| S.No. | Week/Contact Hours | Topic | Mode of Delivery |
|---|---|---|---|
| 1 | Week 1 (2 contact Hours) | Hardware modeling with the Verilog HDL-Introduction, | **Lecture using online presentation and power point presentation** |
| 2 | Week 2 (3 contact Hours) | Hardware Encapsulation, Hardware modeling using Verilog primitives-descriptive style, structural description, | |
| 3 | Week 3 (3 contact Hours) | Hardware modeling using Verilog primitives, Behavioural Description, Hierarchical description, | |
| 4 | Week 4 (2 contact Hours) | Logic System, Datatypes, Operators in Verilog HDL, | |
| 5 | Week 4 (1 contact Hour) | **ASSESSMENT I** | **Online quiz** |
| 6 | Week 5 (3 contact Hours) | Verilog Models of gate propogation delay, net delays, Modules and path delay, | **Lecture using online presentation and power point presentation** |
| 7 | Week 6 (3 contact Hours) | Inertial delay effects and pulse rejection, Behavioural Descriptions- Behavioral statements | |

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|---|---|---|---|
| 8 | Week 7 | **ASSESSMENT II** | **Descriptive/Numerial (Written)** |
| 9 | Week 8 (3 contact Hours) | Intra assessment delay, constructs | **Lecture using online presentation and power point presentation** |
| 10 | Week 9 (3 contact Hours) | Behavioural description-system task,behavioural model of FSM Synthesis of combinational logic-HDL based sysnthesis | **Lecture using online presentation and power point presentation** |
| 11 | Week 10 (3 contact Hours) | Synthesis of combinational logic-styles for sysnthesis Synthesis of sequential logic-latches shift registers,counters | |
| 12 | Week 11 | **ASSESSMENT III** | **Descriptive/Numerial (Written)** |
| 13 | Week 12 (3 contact Hours) | Synthesis of sequential logic-synthesis of FSM. Synthesis of language constructs-nets, variables, | **Lecture using online presentation and power point presentation** |
| 14 | Week 13 (3 contact Hours) | Synthesis of language constructs – expressions and operators, assignments and compiler directives | |
| 15 | Week 14 (1 contact Hour) | **ASSESSMENT IV** | **Online quiz** |
| 16 | Week 14 (2 contact Hours) | Switch level models, Design examples | **Lecture using online presentation and power point presentation** |
| 17 | Week 15 | **END ASSESSMENT** | **Descriptive/Numerical (Written)** |

**COURSE ASSESSMENT METHODS**

| S.No. | Mode of Assessment | Week/Date | Duration | % Weightage |
|---|---|---|---|---|
| | | | | |
| 1 | Assessment I (Quiz) | 1st week of Oct | (30 minutes) | 15% |
| 2 | Assessment II | 3rd Week of Oct | (60 minutes) | 20% |
| 3 | Assessment III (Quiz) | 4th Week of Nov | (60 minutes) | 20% |
| 4 | Assessment IV | 2nd Week of Dec | (30 minutes) | 15% |
| CPA | Assessment V (CPA) | 2nd Week of Dec | (60 minutes) | 20% |
| 6 | End Assessment | 4th Week of Dec | (180 minutes) | 30% |

**COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)**

1. Feedback from the students during class committee meeting.
2. Queries through questionnaire.

**COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)**

**ATTENDANCE**

1. Attendance will be taken by the faculty in all the contact hours. Every student should try to be present in the class during these contact hours.

**COMPENSATION ASSESSMENT**

1. Attending all the assessments are MANDATORY for every student.
2. Every student is expected to score minimum 40% of the maximum mark of the class in the total assessment (1, 2, 3, 4 and 6) to pass the course. Otherwise the student would be declared fail and 'F' grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.
3. Those students who missed any of the continuous assessments (CAs) due to genuine reasons can appear for retest. The scores in the retest will be taken into account for computing marks for CA.

**ACADEMIC HONESTY & PLAGIARISM**

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any Assessments is considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

**ADDITIONAL INFORMATION**

Queries and feedback may also be emailed to the Course Faculty at **sarchana@nitt.edu**

**FOR APPROVAL**

**Course Faculty: (Archana S)** **CC-Chairperson** _____ **HOD** _____