DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	**M-Tech in Electronics & Communication Engineering /VLSI System**		
Course Title	**Digital System Design**		
Course Code	**EC661**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**None**		
Session	**July 2021**	**Section (if, applicable)**	
Name of Faculty	**Dr. Varun P. Gopi**	**Department**	**ECE**
Email	**varun@nitt.edu**	**Telephone No.**	**+919995114547**
Name of Course Coordinator(s) (if, applicable)	**Dr. Varun P. Gopi**		
E-mail	**varun@nitt.edu**	**Telephone No.**	**+919995114547**
Course Type	**Elective course**		

Syllabus (approved in BoS)

Unit1: Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.

Unit2: Combinational network delay. Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis.

Unit3: Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers

Unit4: Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.

Unit 5: Reconfigurable Computing-Fine grain and Coarse grain architectures, Configuration Architectures-Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing

Text Books

1. N.H.E. Weste, D. Harris, "CMOS VLSI Design (4thedition)", Pearson, 2010.
2. W. Wolf, "FPGA-based System Design", Pearson, 2004.
3.S. Hauck&A.DeHon, "Reconfigurable computing: the theory and practice of FPGA-based computation", Elsevier, 2008

Reference Books

1.F.P. Prosser & D. E. Winkel, "Art of Digital Design", 1987.
2.R.F.Tinde, "Engineering Digital Design", (2nd edition), Academic Press, 2000.
3.C. Bobda, "Introduction to reconfigurable computing", Springer, 2007.
4.M.Gokhale&P.S.Graham,"Reconfigurable computing: accelerating computation with field-programmable gate arrays", Springer, 2005.
5.C.Roth," Fundamentals of Digital Logic Design", Jaico Publishers, 5thedition., 2009.
6.Recent literature in Digital System Design.

COURSE OBJECTIVES

1. To get an idea about designing complex, high speed digital systems and how to implement such design.

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
1. Identify mapping algorithms into architectures	1,2,3
2. Summarize various delays in combinational circuit and its optimization methods.	1,2,3
3. Summarize circuit design of latches and flip-flops	1,2,3
4. Construct combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.	1,2,3
5. Summarize the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable	1,2,3

COURSE PLAN – PART II

COURSE OVERVIEW

This course gives you a complete insight into the modern design of digital systems fundamentals from an eminently theoretical point of view. This approach focus on foundation for the design of complex digital systems.

COURSE TEACHING AND LEARNING ACTIVITIES

S. No	Week/Contact Hours	Topic	Mode of Delivery
1	**2 to 6 August (3 contact hours)**	Mapping algorithms into Architectures: Data path synthesis.	
2	**9 to 13 August (3 contact hours)**	Control structures, critical path and worst case timing analysis.	
3	**16 to 20 August (3 contact hours)**	FSM & Hazards	

4	**23 to 27 August (3 contact hours)**	Combinational network delay. Power and energy optimization in combinational logic circuit.	C&T, PPT, group discussion, Quizzes, assignments
5	**30 August to 3 September (3 contact hours)**	Sequential machine design styles.	
6	**6 to 9 September (3 contact hours)**	Rules for clocking. Performance analysis	
7	**13 to 17 September (3 contact hours)**	Sequencing static circuits. Circuit design of latches and flip-flops.	
8	**20 to 24 September (3 contact hours)**	Static sequencing element methodology.	
9	**27 to 28 September (3 contact hours)**	Sequencing dynamic circuits. Synchronizers.	
10	**4 to 8 October (3 contact hours)**	Data path and array subsystems: Addition / Subtraction,	
11	**11 to 14 October (3 contact hours)**	Comparators, counters, coding, multiplication and division.	
12	**18 to 22 October (3 contact hours)**	SRAM, DRAM, ROM, serial access memory, context addressable memory.	
13	**25 to 29 October (3 contact hours)**	Reconfigurable Computing-Fine grain and Coarse grain architectures,	
14	**1 to 5 November (3 contact hours)**	Configuration architectures-Single context, Multi context, partially reconfigurable.	
15	**8 to 12 November (3 contact hours)**	Pipeline reconfigurable, Block Configurable, Parallel processing.	

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

	Mode of Assessment	**Week/Date**	**Duration**	**% Weightage**
1	Assignment 1	3th Week		5

2	Close book (Descriptive Type Examination)	5th Week	60 Minutes	20
3	Assignment 2	8th Week		5
4	Close book (Descriptive Type Examination)	10th Week	60 Minutes	20
CPA	Compensation Assessment*	12th Week	60 minutes	Please refer course policy for more details
5	Quiz	13th Week	30 Minutes	20
6	Final Assessment *	15th Week	180 Minutes	30

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. The students through class representative may give their feedback at any time which will be duly addressed.
2. Feedback from the students through MIS and class committee meetings

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)

All the students are advised to come to the class regularly. All the correspondence (schedule of classes/ schedule of assignment/ course material/ any other information regarding this course) will be intimated in the class as well as in group mail.

COMPENSATION ASSESSMENT POLICY

If any student who fails to attend assessment 2 or assessment 4 due to any genuine reasons, student is permitted to attend compensation assessment for the weightage of 20 % (Including assessment 2 & assessment 4 Portions)

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**
- Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying

from others during an assessment will be treated as punishable dishonesty.

- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

The faculty is available for consultation at times as per the intimation given by the faculty

FOR APPROVAL

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____

Dr. Varun P. Gopi

Guidelines:

a) **The number of assessments for a course shall range from 4 to 6.**

b) **Every course shall have a final assessment on the entire syllabus with at least 30% weightage.**

c) **One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered. Details of compensation assessment to be specified by faculty.**

d) **The passing minimum shall be as per the regulations.**

e) **Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.**

f) **Absolute grading policy shall be incorporated if the number of students per course is less than 10.**

g) **Necessary care shall be taken to ensure that the course plan is reasonable and is objective.**