

**NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI**

This course outline template acts as a guide for writing your course outline. As every course is different, please feel free to amend the template/ format to suit your requirements.

<b>COURSE OUTLINE TEMPLATE</b>			
<b>Course Title</b>	<b>HDL Programming Laboratory</b>		
<b>Course Code</b>	<b>EC655</b>	<b>No. of Credits</b>	<b>2</b>
<b>Department</b>	<b>ECE</b>	<b>Faculty</b>	<b>Dr. R. K. Kavitha</b>
<b>Pre-requisites Course Code</b>	<b>None</b>		
<b>Course Coordinator(s) (if, applicable)</b>			
<b>Other Course Teacher(s)/Tutor(s) E-mail</b>	<b>rkkavitha@nitt.edu</b>	<b>Telephone No.</b>	<b>0431-2503322</b>
<b>Course Type</b>	<input checked="" type="checkbox"/> <b>Lab course</b> <input type="checkbox"/> <b>Elective course</b>		
<b>COURSE OVERVIEW</b>			
This course will Introduce Fundamentals of HDL programming			
<b>COURSE OBJECTIVES</b>			
<ul style="list-style-type: none"> <li>• To design combinational, sequential circuits using Verilog HDL.</li> <li>• To verify and design the digital circuit by means of Computer Aided Engineering tools which involves in programming with the help of Verilog HDL.</li> </ul>			
<b>COURSE OUTCOMES (CO)</b>			
<b>Course Outcomes</b>	<b>Aligned Programme Outcomes (PO)</b>		
After successful completion of the course the students are able to			
CO1: understand the basic concepts of verilog HDL	PO1 -H PO2,PO5-M PO3,PO5-L		
CO2: model digital systems in verilog HDL at different levels of abstraction	PO1-H PO2,PO3,PO5-M PO4,PO9-L		
CO3: know the simulation techniques and test bench creation.	PO1,PO2,PO3-H PO4,PO5-M PO5,PO9-L		
CO4: understand the design flow from simulation to synthesizable version	PO2,PO3-H PO1,PO4-M PO5,PO7,PO9-L		
CO5: get an idea of the process of synthesis and post-synthesis	PO2,PO3,PO9-H PO1,PO4,PO5-M PO7-L		
	H-High M- Medium L=Low		

## COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
1.	2 <sup>nd</sup> week of September	Lab course Introduction and Tool Flow Demo	Online Mode through <b>MS Team</b> Plat form
2.	3 <sup>rd</sup> & 4 <sup>th</sup> week of September	Adder/ Subtractor	
3.	First week of October	Multiplexer/ Demultiplexer	
4.	Second week of October	Encoder/ Priority Encoder	
5.	Third week of October	Code Converter	
6.	Fourth week of October	Flipflop	
7.	First week of November	Shift Register/ Universal Shift Register	
8.	Second week of November	Comparator, Upcounter/ Downcounter	
9.	Third week of November	Udps	
10.	Fourth week of November	Memory – ROM, RAM	
11.	First week of December	Array Multiplier/ Array Multiplier With Pipelining	
12.	2 <sup>nd</sup> week of December	FIR Filter/ Fir Filter With Pipelinig	
13.	3 <sup>rd</sup> week of December	Project Demo	

## COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Continuous Assessment			20 marks
2.	Written test (Assessment 1)	December First week	1 Hour	30 marks
3.	Mini Project	December second week	1 Hour	20 marks
4.	End Sem Exam	As per the Academic Calender	3 Hours	30 marks
	Compensation Assessment	Not Applicable for Labs	-	-

**ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc****Text Books:**

- 1. M.D.Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, PHI, 1999.
- 2. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson, 2003.

**Reference Books:**

- J Bhaskar, “A Verilog HDL Primer (3rd edition)”, Kluwer, 2005.
- M.G.Arnold, “Verilog Digital – Computer Design”, Prentice Hall (PTR), 1999.
- Recent literature in Modeling and Synthesis with Verilog HDL.

-3-

**COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)****Course feedback is assessed through**

1. Class committee meeting
2. Performance in the assessments
3. Course exit survey form

**Course Attainment is calculated through**

1. Direct tools (Exams and seminars)

**COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)**

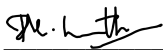
1. The students through class representative may give their feedback at any time which will be duly addressed.
2. Feedback from the students through MIS and class committee meetings.

**ADDITIONAL COURSE INFORMATION**

Any queries send a mail to [rkkavitha@nitt.edu](mailto:rkkavitha@nitt.edu)

**FOR SENATE'S CONSIDERATION**

Course Faculty



CC-Chairperson



HOD

