

**NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI**

This course outline template acts as a guide for writing your course outline. As every course is different, please feel free to amend the template/ format to suit your requirements.

<b>COURSE OUTLINE TEMPLATE</b>			
<b>Course Title</b>	<b>BASICS OF VLSI</b>		
<b>Course Code</b>	<b>EC653</b>	<b>No. of Credits</b>	<b>3</b>
<b>Department</b>	<b>ECE</b>	<b>Faculty</b>	<b>Dr. R. K. Kavitha</b>
<b>Pre-requisites Course Code</b>	<b>None</b>		
<b>Course Coordinator(s) (if, applicable)</b>			
<b>Other Course Teacher(s)/Tutor(s) E-mail</b>	<b>rkkavitha@nitt.edu</b>	<b>Telephone No.</b>	<b>0431-2503322</b>
<b>Course Type</b>	<input checked="" type="checkbox"/> <b>Core course</b> <input type="checkbox"/> <b>Elective course</b>		
<b>COURSE OVERVIEW</b>			
This course will Introduce fundamental concepts and various aspects of VLSI			
<b>COURSE OBJECTIVES</b>			
<ul style="list-style-type: none"> <li>. To provide rigorous foundation in MOS and CMOS digital circuits</li> <li>To train the students in transistor budgets, clock speeds and the growing challenges of power consumption and productivity</li> </ul>			
<b>COURSE OUTCOMES (CO)</b>			
<b>Course Outcomes</b>	<b>Aligned Programme Outcomes (PO)</b>		
After successful completion of the course the students are able to			
CO1: Implement the logic circuits using MOS and CMOS technology.	PO1 -H PO2,PO5-M PO3,PO5-L		
CO2: Analyze various circuit configurations and their applications	PO1-H PO2,PO3,PO5-M PO4,PO9-L		
CO3: Analyse the merits of circuits according to the technology and applications change.	PO1,PO2,PO3-H PO4,PO5-M PO5,PO9-L		
CO4: Design low power CMOS VLSI circuits.	PO2,PO3-H PO1,PO4-M PO5,PO7,PO9-L		
CO5: Understand the rapid advances in CMOS Technology	PO2,PO3,PO9-H PO1,PO4,PO5-M PO7-L		
	H-High M- Medium L=Low		

<b>COURSE TEACHING AND LEARNING ACTIVITIES</b>			
<b>S.No.</b>	<b>Week</b>	<b>Topic</b>	<b>Mode of Delivery</b>
1.	2 <sup>nd</sup> week of September	Family of digital ICs. Speed / power performance of various IC techniques.	Online Mode through <b>MS Team</b> Plat form
2.	3 <sup>rd</sup> & 4 <sup>th</sup> week of September	MOS transistor structure Nmos & pmos switch concept Compound gates, Pass transistors & Transmission gates Tristate inverters. Multiplexers Latches & Flip flops	
3.	First week of October	Gate layout & Stick diagrams VLSI design flow	
4.	Second week of October	Ideal I-V characteristics of the MOS transistor C-V characteristics. MOS capacitance models	
5.	Third week of October	Non ideal I-V effects (velocity saturation, Sub threshold conduction...) CMOS inverter DC characteristics curve Ratioed inverters transfer function Pass transistor DC characteristics	
6.	Fourth week of October	Switch level RC delay models NAND & NOR gates delay estimation Linear delay model Delay in multistage logic networks	
7.	First week of November	Power dissipation. (Static & dynamic) Resistance & capacitance estimation Delay in distributed RC circuits. (L, T & $\pi$ models)	
8.	Second week of November	Design margins. Hard & soft errors Estimating the logical effort & parasitic delay in Compound gates Hi skew & low skew gates	
9.	Third week of November	Ratioed circuits ( Pseudo- nmos) Pre charge & Evaluation mode of operation of dynamic circuits Domino logic, Multiple output domino logic	
10.	Fourth week of November	Differential logic circuits (DCVS, DSL & DCVSPG) Race problems in dynamic logic circuits	

11.	First week of December	Problem solving BiCMOS inverter Comparison of circuit families Problem solving	
12.	2 <sup>nd</sup> week of December	Integrated resistors & capacitors Integrated resistors & capacitors, Layout design rules Demo on DRC and LVS	Students seminar using PPT
13.	3 <sup>rd</sup> week of December	Comparison of circuit families Problem solving Seminar on Active and passive inductance Demo on processing techniques Conclusion Planar processes, Design rule checkers & circuit extraction n-well & p-well process	Students seminar using PPT

#### COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Written test (Assessment 1) (Descriptive type)	As per the Academic Calender	1 Hour	20 marks (1 ½ units)
2.	Written test (Assessment 2) (Descriptive type)	As per the Academic Calender	1 Hour	20 marks (1 ½ units)
3.	Assignment1/Seminar	November (Four weeks)	-	10 marks (2 units)
4.	Assignment 2 and Problem solving Test	December second week	1 Hour	10+ 10 = 20 marks
5.	Written Exam (Descriptive type)	As per the Academic Calender	3 Hours	30 marks (5 units)
	Compensation Assessment (Only for Assessment 1&2 )	November first week (For <b>genuine reasons</b> only)	1 Hour	20 marks (3 units)

#### ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

##### **Text Books:**

- N.H.E.Weste, D. Harris, "CMOS VLSI Design (3/e)", Pearson, 2005.
- J.Rabey, M. Pedram, "Digital Integrated circuits (2/e)", PHI, 2003.

##### **Reference Books:**

- Pucknell & Eshraghian, "Basic VLSI Design", (3/e), PHI, 1996.
- Logical Effort: Designing Fast CMOS Circuits, Morgan Kaufmann; First edition ,1999)
- Recent literature in Basics of VLSI.

**COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)**

**Course feedback is assessed through**

1. Class committee meeting
2. Performance in the assessments
3. Course exit survey form

**Course Attainment is calculated through**

1. Direct tools (Exams and seminars)

**COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)**

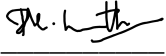
1. The students through class representative may give their feedback at any time which will be duly addressed.
2. Feedback from the students through MIS and class committee meetings.

**ADDITIONAL COURSE INFORMATION**

Any queries send a mail to [rkkavitha@nitt.edu](mailto:rkkavitha@nitt.edu)

**FOR SENATE'S CONSIDERATION**

Course Faculty



CC-Chairperson



HOD

