NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN			
Course Title	**ANALOG IC Design**		
Course Code	**EC651**	**No. of Credits**	**03**
Department	**Electronics and Communication Engineering**	**Faculty**	**Dr. B Venkataramani**
Pre-requisites Course Code	**-**		
Course Coordinator	**-**		
Other Course Teacher(s)/Tutor(s) E-mail		**Telephone No.**	bvenki@nitt.edu **7708977953 0431 2503303**
Course Type	**Program Core**		

COURSE OVERVIEW

This course develops the expertise to draw the equivalent circuits for single stage and multistage amplifiers using MOS. The effect of different types of loads on the performance is studied. The evaluation of the frequency response of the circuits and the application of different types of feedback on MOS amplifiers are studied. The different sources of noise in MOS circuits and computation of noise in MOS amplifiers is studied. The implementation of switched capacitor circuits, current mirrors and bandgap reference are also introduced

COURSE OBJECTIVES

To develop the expertise for designing and analysing the MOS analog VLSI circuits including single stage and multistage amplifiers with and without feedback and with different types of loads

COURSE OUTCOMES (CO)

Students are able to

- CO1: To design single stage MOS amplifiers and analyse its performance
- CO2: To design and understand the operation of differential amplifiers, Compute the common mode and differential gain, and evaluate the effect of mismatches and different loads
- CO3: Study and implementation of two stage MOS operational amplifiers and techniques for gain enhancement and common mode feedback
- CO4: Study and understand switched capacitor based circuits , their imperfections and remedies. Study and realise bandgap reference circuits, current mirrors
- CO5: Study and analyse the frequency response of MOS amplifiers and the effect of feedback on MOS amplifiers. : Study and analyse the noise in single stage and multistage amplifiers

COURSE TEACHING AND LEARNING ACTIVITIES			
S.No.	Week	Topic	Mode of Delivery
1.	6-9 SEP 2021 Week 1 (2 Contact Hours)	Applications of Analog VLSI, Its challenges, MOS I/V Characteristics, Second Order effects,	Lecture C&T/ PPT or any suitable mode
2.	Week 2 & 3 SEP (6 Contact Hours)	MOS Device models, Single Stage Amplifiers – Basic Concepts,	
3.	Week 4 (3 Contact Hours)	Common Source Stage with different loads	
4.	Week 5 (3 Contact Hours)	CS Amplifier with diode connected load & source degeneration	
5.	**Week 5**	**ASSESSMENT - 1 10 Marks**	Assignment
6.	Week 6 & 7 (4 Contact Hours)	CD and CG amplifiers, Cascode Amplifiers. Differential Amplifiers, Differential Pair with MOS loads	
7.	Week 8 21-26 OCT	**ASSESSMENT II - 30 Marks 90 Minutes**	Descriptive/Numerical
8.	Week 9 (3 Contact Hours)	Single Ended and Differential Operation, Basic Differential Pair Differential and Common-Mode Response,	Lecture C&T/ PPT or any suitable mode
9.	Week 10 (3 Contact Hours)	Gilbert Cell, Passive current Mirrors, Basic and Cascode Current mirrors, Active Current Mirrors	
10.	Week 11 (3 Contact Hours)	Frequency Response of Amplifiers – General Considerations, CS amplifier,	
11.	Week 12 23-26 NOV	**ASSESSMENT III - 30 Mark 90 Minutes**	Descriptive/Numerical
12.	Week 13 (3 Contact Hours)	CD and CG amplifiers Cascode Stage, Differential Pair.	Lecture C&T/ PPT or any suitable mode
13.	Week 13 (3 Contact Hours)	Feedback Amplifiers – General Considerations, Feedback Topologies, Effect of Loading	
14.	Week 14 (3 Contact Hours)	Single & Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection,	
15.	**(3 Contact Hours)**	**END ASSESSMENT – 40 Marks**	Descriptive/Numerical

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Assessment I Numerical	5th week	2 days	10
2.	Assessment II Descriptive/Numerical	21-26 OCT 2021	90 Minutes	30
3.	Assessment III Descriptive/Numerical	23-26 NOV 2021	90 Minutes	30
4.	Assessment IV (CPA)	3rd week of DEC 2021	90 Minutes	30
5	End Assessment	4th Week of DEC 2021	180 Minutes	30

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

Text Books

Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Edition 2016.

References:

David A. Johns and Ken Martin, Analog Integrated Circuit Design, Wiley, 1997.

R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, Wiley, (3/e), 2010.

Philip.E.Allen, et al. CMOS Analog Circuit Design, Oxford University Press, 2002.

Paul. R.Gray, et al. Analysis and Design of Analog Integrated Circuits, Wiley, (5/e), 2009.

COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

CORRESPONDENCE

1. All the students are advised to check their NITT WEBMAIL/group mail/suggested by the course faculty, class representative regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through them only.
2. Queries (if required) to the course teacher shall only be emailed to the email id specified by the teacher.

ATTENDANCE

3. Attendance will be taken in all the contact hours automatically by the on line lecture s/w. Every student should try to be present in the class during these contact hours.
4. Those students who missed any of the continuous assessments (CAs) due to genuine reasons can appear for retest . The scores in the retest will be taken into account for computing marks for CA.

ASSESSMENT

5. Every student is expected to score minimum 40% of the maximum mark of the class in the total assessment (1, 2, 3 and 4) to pass the course. Otherwise the student would be declared fail and 'F' grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any assessments is considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL COURSE INFORMATION

FOR SENATE'S CONSIDERATION

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____