DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	**Electronic Design Automation tools**		
Course Code	**EC 654**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**None**		
Session	**Jan.2021**	**Section (if, applicable)**	**Nil**
Name of Faculty	**R.K.Kavitha**	**Department**	**E.C.E**
Email	**rkkavitha@nitt.edu**	**Telephone No.**	**0431-2503322**
Name of Course Coordinator(s) (if, applicable)	**NIL**		
E-mail	**-**	**Telephone No.**	**-**
Course Type	**Core Course**	[■]	

Syllabus (approved in BoS)

OS Architecture: System settings and configuration. Introduction to UNIX commands Handling directories, Filters and Piping, Wildcards and Regular expression, Power Filters and Files Redirection. Working on Vi editor, Basic Shell Programming, TCL Scripting language.

Circuit simulation using Spice - circuit description. AC, DC and transient analysis. Advanced spice commands and analysis. Models for diodes, transistors and opamp. Digital building blocks. A/D, D/A and sample and hold circuits. Design and analysis of mixed signal circuits.

Synthesis and simulation using HDLs-Logic synthesis using Verilog. Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation.

System Verilog- Introduction, Design hierarchy, Data types, Operators and language constructs. Functional coverage, Assertions, Interfaces and test bench structures.

Analog/Mixed Signal Modelling and Verification: Analog/Mixed signal modelling using Verilog-A and Verilog-AMS. Event Driven Modelling: Real number modelling of Analog/Mixed blocks modelling using Verilog-RNM/System Verilog. Analog/Digital Boundary Issues: boundary issues coverage

COURSE OBJECTIVES:

To make the students exposed to Front end and Back end VLSI CAD tools.

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned Programme Outcomes (PO)**
After successful completion of the course the students are able to	

1. execute the special features of VLSI back end and front end CAD tools and UNIX shell script	**a,b,c,d,e**
2. **write Pspice code for any electronics circuit and to perform monte-carlo analysis and sensitivity/worst case analysis.**	**a,b,c,d,e**
3. **design synthesizable Verilog and VHDL code.**	**a,b,c,d,e**
4. **explain the difference between Verilog and system Verilog and are able to write system Verilog code.**	**I,j,k**
5. Model Analog and Mixed signal blocks using Verilog A and Verilog AMS	**I,j,k**

COURSE PLAN – PART II

COURSE OVERVIEW

Digital design flow regardless of technology is a fully automated process. Design flow consists of several steps and there is a need for a toolset in each step of the process. EDA for electronics has rapidly increased in importance with the continuous scaling of semiconductor technology. Design-service companies who use EDA software to evaluate an incoming design for manufacturing readiness. EDA tools are also used for programming design functionality into FPGAs.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1.	**1.**	Course Introduction	**PPT through Online mode**
2.	**2.**	Introduction to UNIX commands	
3.	**3.**	Handling directories, Filters and Piping, Wildcards and Regular expression	
4.	**4.**	Power Filters and Files Redirection	
5.	**5.**	Working on Vi editor	
6.	**6.**	Basic Shell Programming, TCL Scripting language.	

		UNIT II	
7.	**7.**	Circuit simulation using Spice - circuit description. AC, DC and transient analysis	
8.	**8.**	Advanced spice commands and analysis.	
9.	**9.**	Advanced spice commands and analysis.	
10.	**10.**	Models for diodes, transistors and opamp.	
11.	**11.**	Digital building blocks. A/D, D/A Converters	
12.	**12.**	Sample and hold circuits. Design and analysis of mixed signal circuits.	
13.	**13.**	Problem solving using Pspice	
14.		**Assessment –I** **Cycle Test 1**	
		UNIT III	
15.	**14.**	Synthesis and simulation using HDLs	**PPT**
16.	**15.**	Logic synthesis using Verilog.	
17.	**16.**	Logic synthesis using Verilog.	
18.	**17.**	FSM synthesis.	

19.	**18.**	Performance driven synthesis	
20.	**19.**	Types of simulation	
21.	**20.**	Static timing analysis. Formal verification.	
22.	**21.**	Switch level and transistor level simulation	
		UNIT IV	
23.	**22.**	System Verilog- Introduction	**PPT**
24.	**23.**	Design hierarchy	
25.	**24.**	Data types	
26.	**25.**	Operators and language constructs	
27.	**26.**	Functional coverage	
28.	**27.**	Assertions, Interfaces and test bench structures.	
29.		**Assessment-II** **Cycle Test-II**	
		UNIT V	
30.	**28,29**	Analog/Mixed Signal Modelling and Verification-Introduction	**PPT**

31.	**30,31**	Analog/Mixed signal modelling using Verilog-A	
32.	**32,33**	Analog/Mixed signal modelling using Verilog-AMS	
33.	**34,35**	Event Driven Modelling: Real number modelling of Analog/Mixed blocks modelling	
34.	**36,37**	Analog/Digital Boundary Issues: boundary issues coverage	
35.		**End Semester**	

Text Books

1. *M.J.S.Smith, "Application Specific Integrated Circuits",Pearson, 2008.*
2. *S.Sutherland, S. Davidmann, P. Flake, "System Verilog For Design",(2/e), Springer,2006.*

Reference Books

1. *H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999*
2. *Z. Dr Mark, "Digital System Design with System Verilog ",Pearson, 2010.*

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment– 1 (Descriptive Type)	**As per the Academic Calender schedule**	1 hour	**20**
2	Assessment– 2 (Descriptive Type)		1 hour	**20**
3	Assessment - 3 (Assignments & Seminars)			**10**
4	Assessment 4* Surprise Test		1 hour	**20**
CPA	Compensation Assessment*		1hour	**20**
4	Final Assessment *		3 hour	**30**

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Course Exit Survey would be taken at the last working day.

1. The students through class representative may give their feedback at any time which will be duly addressed.
2. Feedback from the students through MIS and class committee meetings.

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, , academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

1. All the students are advised to come to the class regularly. All the correspondence

(schedule of classes/ schedule of assignment/ course material/ any other information regarding this course) will be intimated in the class only.

ATTENDANCE

1. Attendance will be taken by the faculty. 100 % is a mandatory. However, the relaxation upto 20% will be given for leave on medical, and other essential requirements followed in the institute. Every student should maintain minimum 80% physical attendance in these contact hours along with assessment criteria to attend the end semester examination.
2. Any student who fails to maintain 80% and misses any lab experiment needs to appear for the compensation classes with regular evaluation process. Students attendance is compulsory for end semester.
3. Students not having 80% minimum attendance with compensation at the end of the semester will have to REDO the course.

COMPENSATION ASSESSMENT

1. Attending all the assessments are mandatory for every student.
2. Any student who fails to attend the any one of the **Assessment-1,2,3,** Compensation Assessment is allowed **only for genuine reasons. Assessment 4 and End sem are Mandatory.**
3. **Finally every student is expected to score minimum 40 Marks** (including all assessments) to pass the course. Otherwise student would be declared fail and 'F' grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.

ACADEMIC HONESTY & PLAGIARISM

The students are expected to follow institute rules.

ADDITIONAL INFORMATION

FOR APPROVAL

Course Faculty_____ **CC-Chairperson**_____**HOD** _____