DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	**MASTER OF TECHNOLOGY VLSI SYSTEM**		
Course Title	**VLSI SYSTEM TESTING**		
Course Code	**EC652**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**Basics of VLSI**		
Session	**January 2021**	**Section (if, applicable)**	
Name of Faculty	**R.THILAGAVATHY**	**Department**	**ECE**
Email	**thilagavathy@nitt.edu**	**Telephone No.**	**0431-2503313**
Name of Course Coordinator(s) (if, applicable)			
E-mail		**Telephone No.**	
Course Type	☑ **Core course**	☐ **Elective course**	

Syllabus (approved in BoS)

Basics of Testing: Fault models, Combinational logic and fault simulation, Test generation for Combinational Circuits. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation.

Universal test sets: Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

CMOS testing: Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.

Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.

Built-in self-test: Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Text Books:

- Jha & S.D. Gupta, “Testing of Digital Systems”, Cambridge, 2003.
- 2. W. W. Wen, “VLSI Test Principles and Architectures Design for Testability”, Morgan Kaufmann Publishers. 2006.

Reference Books:

- Michael L. Bushnell &Vishwani D. Agrawal," Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits", Kluwar Academic Publishers. 2000.
- P. K. Lala," Digital circuit Testing and Testability", Academic Press. 1997.
- M. Abramovici, M. A. Breuer, and A.D. Friedman, "Digital System Testing and Testable Design", Computer Science Press, 1990.

Preparations for Conducting class and assessments through Online mode

1. The theory classes will be conducted through online mode through MS Teams as per the time table.
2. The course material for the course will be uploaded in MS Teams, which can be downloaded by each student.
3. The online continuous assessments and the final assessment will be conducted online through institute CBT portal.

COURSE OBJECTIVES

To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned Programme Outcomes (PO)**
After successful completion of the course the students are able to	
CO1: Analyse the concepts in testing which can help them design a better yield in IC design.	PO1,PO2,PO3-H PO4,PO5-M PO9-L
CO2: Tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.	PO1,PO2,PO3,PO5,PO7-H PO4,PO9-M
CO3: Describe the various test generation methods for static & dynamic CMOS circuits.	PO2-H PO1,PO5-M PO3,PO4PO9-L
CO4: Explain the design for testability methods for combinational & sequential CMOS circuits.	PO2,PO5-H PO4-M PO1,PO3PO9-L
CO5: Synthesize the BIST techniques for improving testability.	PO2,PO4,PO5-H PO3-M PO1,PO7,PO9-L
	H-High M- Medium L-Low

COURSE PLAN – PART II

COURSE OVERVIEW

This course will Introduce fundamental concepts and various aspects of VLSI testing and Focus on Importance of testing in the design and manufacturing processes. This course will explore Challenges in test generation and fault modeling, Levels of abstraction in VLSI testing. This course may provide overview of VLSI test technology. Students will acquire the knowledge about the following topics:

- Test process and ATE
- Test Economics
- Fault Models
- Fault Simulation
- Testability Measures
- ATPG

• Different Testing Methods (IDDQ, Delay etc.)
• Scan design
• BIST (Built in Self Test)
• Boundary Scan ,Memory test
• Other advanced topics

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1.	Third week of January	Introduction to basic testing principles. Analysis of faults, Test economics, Fault models	PPT
2.	Fourth week of January	Combinational circuit ATPG testing, Sensitized path based testing, Logic simulation	PPT
3.	First week of February	Testability measures (SCOAP), Direct and Indirect Implications, D-Algorithm and PODEM algorithm	PPT
4.	Second week of February	Fault Collapsing and dropping, Serial and parallel fault simulation, Deductive fault simulation, IDDQ testing	PPT
5.	Third week of February	Sequential ATPG and delayed reconvergence, State table method and self-hiding, Extended D - Algorithm	PPT
6.	Fourth week of February	Universal test sets, Pseudo –exhaustive testing, Clocking schemes for delay fault testing	PPT
7.	First week of March	Testability classification for Path delay fault, Test generation for Gate delay fault and segment, delay fault	PPT
8.	Second week of March	Testing dynamic domino circuits, Testing of DCVS circuits, Testing of CMOS static circuits	PPT
9.	Third week of March	Check points and check point transistors, Testing using tree representation	PPT
10.	Fourth week of March	Introduction to fault diagnosis, Cause – effect diagnosis, Effect – cause diagnosis	PPT
11.	First week of April	Scan design testability, Scan cell design for DFT, Scan design flow	Students seminar using PPT
12.	Second week of April	Scan design verification test and cost, Built in self-test (BIST) Architecture	Students seminar using PPT
13.	Third week of April	BIST design rules, LFSR, CA, Signature Analysis, Fault coverage Enhancement	Students seminar using PPT
14.	Fourth week of April	Memory test	Students seminar using PPT

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Assessment -1 (Descriptive type exam-	Fourth week of February	1 ½ Hours	25 marks (1 ½ units)

	Online)			
2.	Assessment -2 (Descriptive type exam-Online)	Fourth week of March	1 ½ Hours	25 marks (1 ½ units)
3.	Assessment – 3 Students seminar presentation + Review of the Research paper	April (Four weeks)	30 minutes(per student)	20 marks (2 units) Unit 4 & 5
CPA	Compensation Assessment*	First week of May (If applicable)	1 ½ Hours	25 marks (3 units) Unit 1,2 & 3
4.	Assessment -4* (Descriptive type exam – online) (Endsemester)	Second week of May	2 Hours	30 marks (All 5 units)

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Course feedback is assessed through

1. Class committee meeting
2. Frequently ask the questions in the class and analyzes the responses
3. Course exit survey form

Course Attainment is calculated through

Direct tools (Exams and Assignments)

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

COURSE ASSESSMENT:

1 Attending all the assessments are MANDATORY for every student.
2 Seminar presentation is MANDATORY for every student within the stipulated time failing which 20% weightage will not be considered for final grade assessment.
3 There will not be any improvement test for the students who score low marks in continuous assessment test.
4 Finally, every student is expected to score minimum marks as per the regulations of the institute out of the total assessments 1,2,3, and 4 to pass the course. Otherwise the student will be declared fail and 'F' grade will be awarded. Further the student can take up only FORMATIVE ASSESSMENT.

MODE OF CORRESPONDENCE (email/ phone etc.)

1 All students are advised to check their NITT webmail/MS Teams account regularly. All the details about the schedule of classes, schedule of assessments, course material and any other information regarding the course will be sent through webmail/MS Teams only.
2 Doubts regarding the course can be clarified through MS Teams by fixing proper timing with the teacher during working hours only.
3 Queries, if any regarding the course shall only through email/MS Teams to the Faculty.

COMPENSATION ASSESSMENT POLICY

1 Any student who fails to maintain 75% attendance only on reasonable medical/official grounds needs to appear for the compensation assessment (CPA) classes.
2 The portion for compensation assessment will be the portion of assessment 1 and 2.
3 There is no CPA for Assessment 3.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**
- Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

ACADEMIC DISHONESTY & PLAGIARISM

1. Sharing the answers through electronic media during online assessments will be treated as dishonesty and it is punishable.
2. Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
3. The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

   The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

Any queries send a mail to thilagavathy@nitt.edu

FOR APPROVAL

Course Faculty R. Thilagavathy ___________ **CC-Chairperson** __ __________ **HOD** _____________