DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the program and specialization	**MTech VLSI Systems, Semester I**		
Course Title	**Modeling and Synthesis with Verilog HDL**		
Course Code	**EC662**	**No. of Credits**	**03**
Course Code of Pre-requisite subject(s)	--		
Session	**Aug 2020**	**Section (if, applicable)**	--
Name of Faculty	**Dr. K. R. Pasupathy**	**ECE Department**	**ECE**
Email	**pasupathy@nitt.edu**	**Telephone No.**	**8754471441**
Name of Course Coordinator	-		
E-mail	--	**Telephone No.**	--
Course Type	**Elective**		

Syllabus (approved in BoS)

- Hardware modelling with the verilog HDL. Encapsulation, modelling primitives, different types of description.
- Logic system, data types and operators for modelling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection.
- Behavioural descriptions in verilog HDL. Synthesis of combinational logic.
- HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.
- Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives. Switch-level models in verilog. Design examples in verilog.

Text Books

1. M.D.Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", PHI, 1999.
2. S. Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", Pearson, 2003.

Reference Books

1. J Bhaskar, "A Verilog HDL Primer", 3rd Edition, Kluwer, 2005.
2. M.G.Arnold, "Verilog Digital – Computer Design", Prentice Hall (PTR), 1999.
3. Recent literature in Modeling and Synthesis with Verilog HDL.

COURSE OBJECTIVES

- To design combinational, sequential circuits using Verilog HDL.
- To understand behavioural and RTL modelling of digital circuits.
- To verify that a design meets its timing constraints, both manually and through the use of computer aided design tools.

- To simulate, synthesize, and program their designs on a development board.
- To verify and design the digital circuit by means of Computer Aided Engineering tools which involves in programming with the help of Verilog HDL.

COURSE OUTCOMES (CO)

At the end of the course student will be able to

1. Understand the basic concepts of verilog HDL.
2. Model digital systems in verilog HDL at different levels of abstraction.
3. Know the simulation techniques and test bench creation.
4. Understand the design flow from simulation to synthesizable version.
5. Get an idea of the process of synthesis and post-synthesis.

COURSE OUTCOMES	**Aligned Programme Outcomes (PO)**
1. Understand the basic concepts of verilog HDL.	**PO1, PO3, PO4, PO5, PO9**
2. Model digital systems in verilog HDL at different levels of abstraction.	**PO1,PO2, PO3, PO4, PO5**
3. Know the simulation techniques and test bench creation.	**PO1,PO2, PO3, PO4,PO5**
4. Understand the design flow from simulation to synthesizable version.	**PO1,PO2, PO3,PO4, PO5**
5. Get an idea of the process of synthesis and post-synthesis.	**PO1, PO4,PO9, PO5**

COURSE PLAN – PART II

COURSE OVERVIEW

To get an idea about designing combinational and sequential circuits using Verilog HDL.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No	**Week/Contact Hours**	**Topic**	**Mode of Delivery**
1.	Week 1 (**3 Contact Hours)**	Hardware modelling with the verilog HDL. Encapsulation.	**Online**
2.	Week 2 **(3 Contact Hours)**	Modelling primitives, different types of description.	**Online**
3.	Week 3 **(3 Contact Hours)**	Logic system, data types and operators for modelling in verilog HDL.	**Online**
4.	Week 4 **(3 Contact Hours)**	Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection.	**Online**
5.	Week 5 **(3 Contact Hours)**	Behavioural descriptions in verilog HDL.	**Online**
6.	Week 6 **(3 Contact Hours)**	Synthesis of combinational logic.	**Online**
7.	Week 7 **(3 Contact Hours)**	HDL-based synthesis - technology-independent design, styles for synthesis of combinational logic.	**Online**

8.	Week 8 **(3 Contact Hours)**	Synthesis of sequential logic.	**Online**
9.	Week 9 **(3 Contact Hours)**	Synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.	**Online**
10.	Week 10 **(3 Contact Hours)**	Synthesis of language constructs, nets, register variables.	**Online**
11.	Week 11 **(3 Contact Hours)**	Expressions and operators, assignments and compiler directives.	**Online**
12.	Week 12 **(3 Contact Hours)**	Switch-level models in verilog. Design examples in verilog.	**Online**

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment I (CT I)	Will be informed in class/ as per institute schedule	90 Minutes	30 %
2	Assessment II (CT II)	Will be informed in class/ as per institute schedule	90 Minutes	30 %
3	Assignments.	Will be informed in class	-	10 %
	Compensation Assessment (CPA)	Will be informed in class	90 Minutes	
4	End Assessment	As per institute schedule	120 Minutes	30 %

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

CORRESPONDENCE

1. All the students are advised to check their NITT WEBMAIL/group mail/suggested by the course faculty, class representative regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through them only.
2. Queries (if required) to the course teacher shall only be emailed to the email id specified by the teacher.

ATTENDANCE

3. Attendance will be taken by the faculty in all the contact hours. Every student should try to be present in the class during these contact hours.
4. **At least 75% attendance is mandatory and maximum of 10% is allowed under on duty (OD) category.**

5. Students with **less than 65% attendance** shall be prevented from writing the final assessment and **shall be awarded V grade**.
6. Those students who missed any of the continuous assessments (CAs) due to genuine reasons can appear for retest. The scores in the retest will be taken into account for computing marks for CA.

ASSESSMENT

7. Attending all the assessments are MANDATORY for every student.
8. Every student is expected to score the minimum marks set by the institute norms in total all assessments to pass the course.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any
   Assessments are considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL INFORMATION

FOR APPROVAL

Pasupathy

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____