DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the program and specialization	**MTech VLSI Systems, Semester I**		
Course Title	**Digital System Design**		
Course Code	**EC661**	**No. of Credits**	**03**
Course Code of Pre-requisite subject(s)	--		
Session	**Aug 2020**	**Section (if, applicable)**	--
Name of Faculty	**Dr. K. R. Pasupathy**	**ECE Department**	**ECE**
Email	**pasupathy@nitt.edu**	**Telephone No.**	**8754471441**
Name of Course Coordinator	-		
E-mail	--	**Telephone No.**	--
Course Type	**Elective**		

Syllabus (approved in BoS)

- Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.
- Combinational network delay. Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis.
- Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.
- Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, content addressable memory.
- Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures- Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.

Text Books

1. N.H.E.Weste, D. Harris, "CMOS VLSI Design, 4th Edition", Pearson, 2010.
2. W.Wolf, "FPGA- based System Design", Pearson, 2004.
3. S.Hauck and A.DeHon, "Reconfigurable computing: the theory and practice of FPGA-based computation", Elsevier, 2008.

Reference Books

1. F.P. Prosser and D. E. Winkel, "Art of Digital Design", 1987.
2. R.F.Tinde, "Engineering Digital Design", 2nd Edition, Academic Press, 2000.
3. C. Bobda, "Introduction to reconfigurable computing", Springer, 2007.
4. M.Gokhale and P.S.Graham, "Reconfigurable computing: accelerating computation with field-programmable gate arrays", Springer, 2005.
5. C.Roth, "Fundamentals of Digital Logic Design", Jaico Publishers, 5th Edition, 2009.

6. Recent literature in Digital System Design.

COURSE OBJECTIVES

- To get an idea about designing complex, high speed digital systems and how to implement such design.

COURSE OUTCOMES (CO)

At the end of the course student will be able to

1. Identify mapping algorithms into architectures.
2. Summarize various delays in combinational circuit and its optimization methods.
3. Summarize circuit design of latches and flip-flops.
4. Construct combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.
5. Summarize the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable.

COURSE OUTCOMES	**Aligned Programme Outcomes (PO)**
1. Identify mapping algorithms into architectures.	**PO1, PO3, PO4, PO9**
2. Summarize various delays in combinational circuit and its optimization methods.	**PO2, PO3, PO4**
3. Summarize circuit design of latches and flip-flops.	**PO2, PO3, PO4**
4. Construct combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.	**PO2, PO3,PO4**
5. Summarize the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable.	**PO1, PO4,PO9**

COURSE PLAN – PART II

COURSE OVERVIEW

To get an idea about designing complex, high speed digital systems and how to implement such design. This involves designing of combinational and sequential circuits with constraints on the inputs signals.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No	**Week/Contact Hours**	**Topic**	**Mode of Delivery**
1.	Week 1 (**3 Contact Hours)**	Mapping algorithms into Architectures: Data path synthesis, control structures.	**Online**
2.	Week 2 **(3 Contact Hours)**	Critical path and worst case timing analysis. FSM and Hazards.	**Online**
3.	Week 3 **(3 Contact Hours)**	Combinational network delay. Power and energy optimization in combinational logic circuit.	**Online**
4.	Week 4 **(3 Contact Hours)**	Sequential machine design styles. Rules for clocking. Performance analysis.	**Online**

5.	Week 5 **(3 Contact Hours)**	Sequencing static circuits. Circuit design of latches and flip-flops.	**Online**
6.	Week 6 **(3 Contact Hours)**	Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.	**Online**
7.	Week 7 **(3 Contact Hours)**	Data path and array subsystems: Addition / Subtraction, Comparators.	**Online**
8.	Week 8 **(3 Contact Hours)**	Counters, coding, multiplication and division.	**Online**
9.	Week 9 **(3 Contact Hours)**	SRAM, DRAM, ROM.	**Online**
10.	Week 10 **(3 Contact Hours)**	Serial access memory, content addressable memory.	**Online**
11.	Week 11 **(3 Contact Hours)**	Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures-Single context, Multi context.	**Online**
12.	Week 12 **(3 Contact Hours)**	Partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.	**Online**

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment I (CT I)	Will be informed in class/ as per institute schedule	75 Minutes	25 %
2	Assessment II (CT II)	Will be informed in class/ as per institute schedule	75 Minutes	25 %
3	Assignments.	Will be informed in class/ as per institute schedule	-	20 %
	Assessment (CPA)	Will be informed in class	75 Minutes	
4	End Assessment	As per institute schedule	120 Minutes	30 %

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

CORRESPONDENCE

1. All the students are advised to check their NITT WEBMAIL/group mail/suggested by the course faculty, class representative regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through them only.
2. Queries (if required) to the course teacher shall only be emailed to the email id specified by the

teacher.

ATTENDANCE

3. Attendance will be taken by the faculty in all the contact hours. Every student should try to be present in the class during these contact hours.
4. **At least 75% attendance is mandatory and maximum of 10% is allowed under on duty (OD) category.**
5. Students with **less than 65% attendance** shall be prevented from writing the final assessment and **shall be awarded V grade**.
6. Those students who missed any of the continuous assessments (CAs) due to genuine reasons can appear for retest. The scores in the retest will be taken into account for computing marks for CA.

ASSESSMENT

7. Attending all the assessments are MANDATORY for every student.
8. Every student is expected to score the minimum marks set by the institute norms in total all assessments to pass the course.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any
   Assessments are considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL INFORMATION

FOR APPROVAL

Pasupathy B. Malemukti

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____