NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE PLAN – PART I			
Course Title	VLSI System Testing - M.Tech. Ist year		
Course Code	**EC652**	**No. of Credits**	**03**
Course Code of Pre-requisite subject(s)	--		
Session	**January 2020**	**Section (if, applicable)**	**NA**
Name of Faculty	**Ms.P.Muthu Krishnammal**	**Department**	**M.Tech (VLSI Systems)**
Email	muthup@nitt.edu	**Telephone No.**	**9884588247**
Name of Course Coordinator	**NA**		
E-mail	--	**Telephone No.**	--
Course Type	**PE**		

Syllabus (approved in BoS)

- Basics of Testing: Fault models, Combinational logic and fault simulation, Test generation for Combinational Circuits. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation
- Universal test sets: Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.
- CMOS testing: Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.
- Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.
- Built-in self-test: Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing

Text Books

1. N. Jha& S.D. Gupta, “Testing of Digital Systems”, Cambridge, 2003.

2. W. W. Wen, "VLSI Test Principles and Architectures Design for Testability", Morgan Kaufmann Publishers. 2006.

Reference Books

1. Michael L. Bushnell &Vishwani D. Agrawal," Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits", Kluwar Academic Publishers. 2000.
2. P. K. Lala," Digital circuit Testing and Testability", Academic Press. 1997.
3. M. Abramovici, M. A. Breuer, & A.D. Friedman, "Digital System Testing and Testable Design", Computer Science Press, 1990. 4. Recent literature in VLSI System Testing.

COURSE OBJECTIVES

To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

COURSE OUTCOMES (CO)

CO1: apply the concepts in testing which can help them design a better yield in IC design.
CO2: tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.
CO3: analyse the various test generation methods for static & dynamic CMOS circuits.
CO4: identify the design for testability methods for combinational & sequential CMOS circuits.
CO5: recognize the BIST techniques for improving testability.

COURSE OUTCOMES	Aligned Programme Outcomes (PO)
1. Apply the concepts in testing which can help them design a better yield in IC design.	PO1, PO2, PO3-H, PO4,PO4-M,PO9-L
2. Tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.	PO1, PO2, PO3, PO5, PO7-HPO4,PO4-M
3. Analyze the various test generation methods for static & dynamic CMOS circuits	PO2-H, PO1, PO5-M PO3,PO4,PO9-L
4. Identify the design for testability methods for combinational & sequential CMOS circuits.	PO2,PO5-H,PO4-M PO1,PO3,PO9-L

5.recognize the BIST techniques for improving testability	PO2, PO5,PO4-H, PO3-M, PO!,PO7,PO9-L

COURSE PLAN – PART II

COURSE OVERVIEW

This course will introduce fundamental concepts and various aspects of VLSI testing and focus on importance of testing in the design and manufacturing processes. This course will explore challenges in test generarion and fault modeling. Levels of abstraction in VLSI testing. This course may provide overview of VLSI test technology. Students will acquire the knowledge about the following topics:

- Test process and ATE
- Test economics
- Fault Models
- Testability measures
- ATPG
- Different testing modules (IDDQ, Delay, etc)
- Scan design
- BIST
- Boundary scan, Memory Test
- Other advanced topics

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1.	Week 1 (3 Contact Hours)	Introduction to basic testing principles, Analysis of faults, Test economics, Fault models	Lecture C&T/ PPT or any suitable mode
2.	Week 2 (3 Contact Hours)	Combinational ATPG testing, Sensitized path based testing, Logic simulation	Lecture C&T/ PPT or any suitable mode
3.	Week 3 (3 Contact Hours)	Testability measures (SCOAP), Direct and indirect implications, D-algorithm and PODEM algorithm.	Lecture C&T/ PPT or any suitable mode
4	Week 4 (3 Contact Hours)	Fault collapsing and dropping, serial and parallel fault simulation, IDDQ testing	Lecture C&T/ PPT or any suitable mode
5.	Week 5 (3 Contact Hours)	Sequential ATPG and delayed reconvergence, state table	Lecture C&T/ PPT or any

		method and self hiding, Extended D-algorithm	suitable mode
6.	Week 6 (3 Contact Hours)	Universal test sets, Pseudo exhaustive testing, Clocking schemes for delay fault testing	Lecture C&T/ PPT or any suitable mode
7	Week 7 (3 Contact Hours)	Testability classification for path delay fault, Test generation for gate delay fault and segment, delay fault	Lecture C&T/ PPT or any suitable mode
8	Week 8 (3 Contact Hours)	Testing dynamic domino circuits, testing of DCVS circuits, testing of CMOS static circuits	Lecture C&T/ PPT or any suitable mode
9.	Week 9 (3 Contact Hours)	Check points and check point transistors, testing using tree representation	Lecture C&T/ PPT or any suitable mode
10	Week 10 (3 Contact Hours)	Introduction to fault diagnosis, cause effect diagnosis	Lecture C&T/ PPT or any suitable mode/seminar
11	Week 11 (3 Contact Hours)	Scan design testability, scan cell design for DFT, scan design flow	Lecture C&T/ PPT or any suitable mode/ seminar
12	Week 12 (3 Contact Hours)	Scan design verification test and cost, BIST architecture	Lecture C&T/ PPT or any suitable mode/seminar
13	Week 13 (3 Contact Hours)	BIST design rules, LFSR, CA, signature analysis, fault coverage enhancement	Lecture C&T/ PPT or any suitable mode/Seminar

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment I (CT I)	3rd week Feb	1 hour	20
2	Assessment II (CT II)	4th week March	1 hour	20
3	Assessment III (seminar/ Assignment)	April Week of March	30 minutes per student (seminar)	10

4	Assessment IV (Endsem	May 1st week	3 Hours	50
5	Assessment V (CPA)	3rd Week of April	60 Minutes	20

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students through MIS and class committee meetings.

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

CORRESPONDENCE

All the students are advised to check their NITT WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be intimated in Class Only.

ATTENDANCE

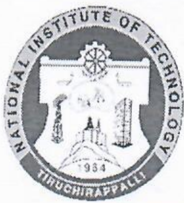
- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**
- Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

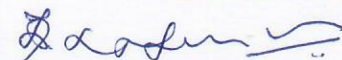
ASSESSMENT

1. Attending all the assessments is MANDATORY for every student.
2. If any student is not able to attend any of the Continuous Assessments due to genuine reason, student is permitted to attend the **compensation assessment*** (CPA) with Corresponding weightage. (This is not valid for students who have attendance lag also.)
3. Please refer institute Regulations/guidelines for grading policy.

ACADEMIC HONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, CC-chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted



to the Academic office. The above policy against academic dishonesty shall be applicable for all the programme.
ADDITIONAL INFORMATION
Queries may also be emailed to the Course Coordinator directly at muthup@nitt.edu
FOR APPROVAL
 **Course Faculty** ___________ **CC-Chairperson** **HOD** Mrs. P. MUTHU KRISHNAMMAL