DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	***B. Tech.*** ***Electronics and Communication Engineering***		
Course Title	***Digital Signal Processors and Applications***		
Course Code	***ECPC20***	**No. of Credits**	***3 (Three)***
Course Code of Pre-requisite subject(s)	*ECPC10 Signals and Systems* *ECPC15 Digital Signal Processing*		
Session	July 2019	**Section (if, applicable)**	*Both A and B*
Name of Faculty	*Dr. M. Bhaskar*	**Department**	*ECE*
Email	*bhaskar@nitt.edu*	**Telephone No.**	*0431-2503310*
Name of Course Coordinator(s) (if, applicable)	*Nil*		
E-mail	---	**Telephone No.**	---
Course Type	☐ **Core course**	☐ **Elective course**	

Syllabus (approved in BoS)

Fixed-point DSP architectures. Basic Signal processing system. Need for DSPs. Difference between DSP and other processor architectures. TMS320C54X, ADSP21XX, DSP56XX architecture details. Addressing modes. Control and repeat operations. Interrupts. Pipeline operation. Memory Map and Buses.
Floating-point DSP architectures. TMS320C3X, DSP96XX architectures. Cache architecture. Floating-point Data formats. On-chip peripherals. Memory Map and Buses.
On-chip peripherals. Hardware details and its programming. Clock generator with PLL. Serial port. McBSP. Parallel port. DMA. EMIF. I2C. Real-time-clock(RTC). Watchdog timer.
Interfacing. Serial interface- Audio codec. Sensors - Humidity/temperature sensor, flow sensor, accelerometer, pulse sensor and finger print scanner. A/D and D/A interfaces. Parallel interface- Memory interface. RF transceiver interface – Wi-Fi and Zigbee modules.
DSP tools and applications. Implementation of Filters, DFT, QPSK Modem, Speech processing. Video processing, Video Encoding/Decoding. Biometrics. Machine Vision. High performance computing (HPC).

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

1 *B.Venkataramani & M.Bhaskar, "Digital Signal Processor, Architecture, Programming and Applications",(2/e), McGraw- Hill, 2010*
2 *S.Srinivasan & Avtar Singh, "Digital Signal Processing, Implementations using DSP Microprocessors with Examples from TMS320C54X", Brooks/Cole, 2004.*
3 *S.M.Kuo & W.S.S.Gan," Digital Signal Processors: Architectures, Implementations, and Applications", Prentice Hall, 2004*
4 *C.Marven & G.Ewers, "A Simple approach to digital signal processing", Wiley Inter science, 1996.*
5 *R.A.Haddad & T.W.Parson, "Digital Signal Processing: Theory, Applications and Hardware", Computer Science Press NY, 1991.*
6 *Texas Instruments (TI) DSP manuals and application notes www.ti.com or www.dspvillage.com*

COURSE OBJECTIVES

Learn the basic differences in the architecture of microprocessors(μPs), microcontrollers(μCs) and digital signal processors (DSPs). Learn the internal architecture blocks of fixed and floating-point digital signal processors (DSPs). Get familiar with programming skills and the techniques to implement signal processing algorithms in DSPs. Real time signal interface and signal processing in DSPs.

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
1. *Learn the architecture details of fixed point DSPs.*	**PO1,PO2**
2. *Learn the architecture details of floating point DSPs*	**PO1,PO2**
3. *Infer about the control instructions, interrupts, pipeline operations, memory and buses.*	**PO1,PO2,PO3,PO4**
4. *Illustrate the features of on-chip peripheral devices and its interfacing with real time application devices.*	**PO4,PO5,PO6,PO11**
5. *Learn to implement the signal processing algorithms and applications in DSPs*	**PO4,PO5,PO6,PO7, PO11**

COURSE PLAN – PART II

COURSE OVERVIEW

To learn the architecture of Fixed point and floating point DSP architectures and its programming details. To learn real time interfacing concepts and to implement real time signal processing algorithms in DSPs.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
1	1st week (3 contact hours)	*Introduction to basics of signal processing, need for signal processing, elements of signal processing, MAC hardware*	*PPT, Chalk and talk*
2	2nd week (3 contact hours)	*Basic difference between processor architectures, key features of DSP processors (TMS320C54X)*	*PPT, Chalk and talk*
3	3rd week (3 contact hours)	*Design of ALU, multiplier and MAC unit for single, dual bus from data memory and single bus from program memory*	*PPT, Chalk and talk*
4	4th week (3 contact hours)	*Design of PLU, ARAU, barrel shift register and memory mapped registers (MMREGS)*	*PPT, Chalk and talk*
5	5th week (3 contact hours)	*Introduction to addressing modes, direct, immediate, indirect, circular, dual operand and parallel addressing modes with examples. Absolute and accumulator addressing modes*	*PPT, Chalk and talk*
6	6th week (3 contact hours)	*Control unit, interrupts and pipeline operation, power down modes. On-chip buses and memory configuration.*	*PPT, Chalk and talk*
7	7th week (3 contact hours)	*On-chip peripherals, clock generator, timer serial port and parallel port, programming and interfacing details*	*PPT, Chalk and talk*
8	8th week (3 contact hours)	*Floating point DSP architecture (TMS320C3X), CPU details*	*PPT, Chalk and talk*

9	9th week (3 contact hours)	Floating point data formats, addressing modes, control unit, interrupts, pipeline operation and power down modes	PPT, Chalk and talk
10	10th week (3 contact hours)	On-chip peripheral, interfacing details. On-chip DMA controllers and its interfacing.	PPT, Chalk and talk
11	11th week (3 contact hours)	Other DSP architectures, A/D, D/A, memory interface and other interface	PPT, Chalk and talk
12	12th week (3 contact hours)	Signal processing applications and tools. FIR filter, DFT, speech processing, modem design	PPT, Chalk and talk

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S. No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assignment - 1 (1st unit)	4th week	One week	5
2	Assesment - 1 (Descriptive exam) (1st and 2nd units)	5th week	1 hour	20
3	Assignment - 2 (5th unit)	10th week	One week	5
4	Assesment - 2 (Descriptive exam) (3rd and 4th units)	11th week	1 hour	20
CPA	Compensation Assesment (Descriptive exam) (1st to 4th units)	12th week	1 hour	20
5	Final Assessment (Descriptive exam) (All units – Endsemester)	3rd week of November	3 hours	50

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. Feedback from students during class committee meetings
2. Feedback through questionnaire at the end of the semester

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

COURSE ASSESSMENT:

1 Attending all the assessments are MANDATORY for every student
2 If any of the student is not able to attend any of the continuous assessment descriptive examination due to genuine reason (any academic related work through department or medical grounds only), student is permitted to attend CPA.
3 Submission of assignments is MANDATORY for every student within the stipulated time failing which 10% weightage will not be considered for final grade assessment
4 There will not be any improvement test for the students who score low marks in continuous assessment test.
5 Finally, every student is expected to score minimum marks as per the regulations of the institute out of the total assessments 1,2,3,4/CPA and 5 to pass the course. Otherwise the student will be declared fail and 'F' grade will be awarded. Further the student can take up only FORMATIVE ASSESSMENT.

MODE OF CORRESPONDENCE (email/ phone etc.)

1 *All students are advised to check their NITT webmail regularly. All the details about the schedule of classes, schedule of assessments, course material and any other information regarding the course will be sent through webmail only.*
2 *Doubts regarding the course can be clarified by fixing proper timing with the teacher during working hours only.*
3 *Queries, if any regarding the course shall only through email to the teacher.*

COMPENSATION ASSESSMENT POLICY

1 *Any student who fails to maintain 75% attendance only on reasonable medical/official grounds needs to appear for the compensation assessment (CPA) classes.*
2 *The portion for compensation assessment will be the portion of assessment 1 and 2.*

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

1. ***At least 75% attendance in each course is mandatory.***
2. ***A maximum of 10% shall be allowed under On Duty (OD) category.***
3. *Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.***

ACADEMIC DISHONESTY & PLAGIARISM

1. *Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.*
2. *Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.*
3. *The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.*

   The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

The faculty is available for consultation at times as per the intimation given by the faculty.

FOR APPROVAL

25/7/2019

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____

(Dr. R. K. Jeyachitra)