**DEPARTMENT OF Electronics & Communication Engineering**

**NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI**

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| **COURSE PLAN – PART I** |
| **Name of the programme and specialization** | **B.Tech., ECE-6th Semester, Section A and B** |
| **Course Title** | VLSI AND EMBEDDED SYSTEM DESIGN LABORATORY |
| **Course Code** | **ECLR16** | **No. of Credits** | **2** |
| **Course Code of Pre-requisite subject(s)** | **ECPC26** | **-** | **-** |
| **Session** | **January 2019** | **Section** **(if, applicable)** | **A,B** |
| **Name of Faculty** | **Dr. Menka** | **Department** | **ECE** |
| **Email**  | **menka@nitt.edu** | **Telephone No.** | **+91-9416794011** |
| **Name of Course Coordinator(s)****(if, applicable)** | **Dr. Menka**  |
| **E-mail**  |  | **Telephone No.** |  |
| **Course Type** |  **Core course Elective course** ✓ |
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| **Tentative list of experiments-** |
| Text books-1. Moris Mano, , 4th Edition <https://docs.google.com/file/d/0B8-drkZsESDnN2NmYTQxYjQtYTMwZi00N2IzLTkxNjgtZjI1NTZiN2FjNDli/edit>
2. Samir palnitkar, ‘Verilog HDL- A guide to digital design and synthesis’, Sunsoft 1999. <https://docs.google.com/file/d/0BzcOJZmBMzv0WEttVmJVY0xWYXM/view>

Websites/Online Materials1. [**https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-111-introductory-digital-systems-laboratory-spring-2006/projects/**](https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-111-introductory-digital-systems-laboratory-spring-2006/projects/)
2. [**http://users.ece.utexas.edu/~ljohn/teaching/ee460m\_lab\_manual.pdf**](http://users.ece.utexas.edu/~ljohn/teaching/ee460m_lab_manual.pdf)
3. [**http://www.iitk.ac.in/eclub/summercamp/Courses/CompArch/Verilog\_lab\_Solutions.pdf**](http://www.iitk.ac.in/eclub/summercamp/Courses/CompArch/Verilog_lab_Solutions.pdf)
4. [**http://www-classes.usc.edu/engr/ee-s/254/ee254l\_lab\_manual/number\_lock\_verilog\_lab/handout\_files/ee254l\_number\_lock\_verilog\_lab.pdf**](http://www-classes.usc.edu/engr/ee-s/254/ee254l_lab_manual/number_lock_verilog_lab/handout_files/ee254l_number_lock_verilog_lab.pdf)
5. [**https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-111-introductory-digital-systems-laboratory-spring-2006/assignments/**](https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-111-introductory-digital-systems-laboratory-spring-2006/assignments/)
6. **www-classes.usc.edu/engr/ee-s/254/ee254l\_lab\_manual/EE254L\_Lab\_Plan.pdf**
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| **COURSE OBJECTIVES** |
|  To make the students understand the fundamentals of complex digital system design.  To train them to apply these to real life project  To train through experiential learning |
| **COURSE OUTCOMES (CO)** |
| **Course Outcomes** | **Aligned Programme Outcomes (PO)** |
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| CO1: To design simple combinational circuitsCO2: To design simple Sequential circuits using VerilogCO3: To design complex circuits using FSM, data path and controlCO4: Parallel processing and pile line structure designing | PO1: To design simple combinational circuitsPO2: To design simple Sequential circuits using VerilogPO3: To design complex circuits using FSM, data path and controlPO4: Parallel processing and pile line structure designing |

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| **COURSE PLAN – PART II** |
| **COURSE OVERVIEW** |
| The course will focus on the digital system design using Verilog. It will cover recent industrial trends as well. Focus will be on how to design high speed digital circuits, optimizing area, power, delay and cost. |
| **COURSE TEACHING AND LEARNING ACTIVITIES** |
| **S.No.** | **Week** | **Topic** | **Mode of Delivery** |
| 1. | 1 | Introduction to the course, current market share and opportunities in digital system design field across the globe, Basic combinational circuits | C&T, PPT, group discussion, peer learning, experiential learning |
| 2. | 2 | Adder, mux, demux,  |
| 3. | 3 | parallel adder/subtractor, encoders, decoders |
| 4. | 4 | Flip flops, Counters, |
| 5. | 5 | registers, memories |
| 6 | 6 | FFT/IFFT simple |
| 7 | 7 | FFT/IFFT pipeline |
| 8 | 8 | Multiplier with different configuration |
| 9 | 9 | Divider with different configuration |
| 10 | 10 | ALU Design  |
| 11 | 11 onwards | Repetition / revision /exam |
| **COURSE ASSESSMENT METHODS (shall range from 4 to 6)** |
| **S.No.** | **Mode of Assessment** | **Week/Date** | **Duration** | **% Weightage** |
| 1 | I (Close book) | 3rd Week of Feb. 2019 | 60 Minutes | 20 |
| 2 | II (Project) | 4th Week of March 2019 | - | 20 |
| 3 | III (Close book- Quiz) | 1st week of April 2019  | 20 minutes | 10 |
| 4 | IV (Continuous evaluation and Record) | NA | - | 20 |
| CPA | Compensation Assessment\* | 3rd Week of April 2019 | 60 Minutes | 20 |
| 5 | Final Assessment \* | 4th Week of April 2019 | 180 Minutes | 30 |
| **\*mandatory; refer to guidelines on page 4** |
| **COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)** |
| Feedback from the students during class committee meetings.Anonymous feedback through questionnaire. |
| **COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)** |
| **MODE OF CORRESPONDENCE (email/ phone etc)**1. All the students are advised to check their mail IDs regularly. All the correspondence(schedule of classes/ schedule of assessment/ course material/ any other informationRegarding this course) will be intimated in Class or mail.**COMPENSATION ASSESSMENT POLICY**1. Compensation exam can only be conducted if the reason is genuine, e.g. unavoidable medical emergency.
2. The candidates are requested to intimate well in time and they need to produce proof for the same
3. The application should come through HoD/Class Chairperson
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| * A maximum of 10% shall be allowed under On Duty (OD) Category.
* Students with lesser than 65% attendance will be prevented from writing the final assessment and shall be awarded ‘V’ grade.
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| **ACADEMIC DISHONESTY AND PLAGIARISM** |
| * Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
* Zero marks to be awarded for thr offenders. For copying from another student, both students get the same penalty of zero mark.
* The departmental disciplinary committee including the course faculty member, PAC chairperson and HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programs. |
| **ADDITIONAL INFORMATION** |
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**Guidelines:**

1. **The number of assessments for a course shall range from 4 to 6.**
2. **Every course shall have a final assessment on the entire syllabus with at least 30% weightage.**
3. **One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered. Details of compensation assessment to be specified by faculty.**
4. **The passing minimum shall be as per the regulations.**
5. **Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.**
6. **Absolute grading policy shall be incorporated if the number of students per course is less than 10.**
7. Necessary care shall be taken to ensure that the course plan is reasonable and is objective.