Dr. E.S. Gopi

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	**DIGITAL ELECTRONICS LABORATORY**		
Course Code	**ECLR11**	**No. of Credits**	**1**
Course Code of Pre-requisite subject(s)	-		
Session	**July - 2019**	**Sem/Section (if, applicable)**	**III - A** 2nd year
Name of Faculty	**Dr. G. Thavasi Raja**	**Department**	**ECE**
Email	**thavasi@nitt.edu**	**Telephone No.**	**0431-2503317**
Name of Course Coordinator(s) (if, applicable)	-		
Course Type	✓ **Core course**	☐ **Elective course**	

Syllabus (approved in BoS)

- Study of logic gates and verification of Boolean Laws.
- Design of adders and subtractors & code converters.
- Design of Multiplexers & Demultiplexers.
- Design of Encoder and Decoder.
- 2bit and 8bit magnitude comparators
- Study of flip-flops.
- Design and implementation of counters using flip-flops
- Design and implementation of shift registers.
- Simulation of adders, subtractors, encoders & decoder using Verilog HDL
- Simulation of counters & shift registers using Verilog HDL

COURSE OBJECTIVES

- To introduce basic postulates of Boolean algebra and shows the correlation between Boolean expressions
- To introduce the methods for simplifying Boolean expressions
- To outline the formal procedures for the analysis and design of combinational circuits and sequential circuits
- To learn combinational and sequentional circuit simulations using Verilog HDL.

COURSE OUTCOMES (CO)	
Course Outcomes	**Aligned Programme Outcomes (PO)**
1. Demonstrate theoretical device/circuit operation in properly constructed digital circuits.	**PO1, PO2, PO4, PO6, PO10**
2. Able to correctly operate standard electronic test equipment digital multi-meters, power supplies to analyze, test, and implement digital circuits.	**PO1, PO2, PO4, PO6, PO10**
3. Able to correctly analyze a circuit and compare its theoretical performance to actual performance.	**PO1, PO2, PO4, PO6, PO10**
4. Able to apply troubleshooting techniques to test digital circuits.	**PO1, PO2, PO4, PO6, PO10**
5. Able to code a given digital logic design in HDL language.	**PO5, PO6, PO10**

COURSE PLAN – PART II

COURSE OVERVIEW

Digital Electronics Laboratory is a required course for freshman students in the ECE degree program. The purpose of the course is to provide students with an understanding of how to analyze, build, and troubleshoot digital circuits. Student should become proficient in using oscilloscopes, signal analyzers, and similar equipment to test digital circuits. In addition students must learn to write well-organized reports using a word processor. Students should also learn current technologies in the area of programmable memories.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1.	I Week	Study of logic gates and verification of Boolean Laws.	Lab
2.	II Week	Design of adders and subtractors & code converters.	Lab
3.	III Week	Design of Multiplexers & Demultiplexers.	Lab
4.	IV Week	Design of Encoder and Decoder.	Lab
5.	V Week	2bit and 8bit magnitude comparators	Lab
6.	VI Week	Study of flip-flops.	Lab
7.	VII Week	Design and implementation of counters using flip-flops	Lab
8.	VIII Week	Design and implementation of shift registers.	Lab

9.	IX Week	Simulation of adders, subtractors, encoders & decoder using Verilog HDL	Lab
10.	X Week	Simulation of counters & shift registers using Verilog HDL	Lab

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date (tentatively)	Duration	% Weightage
1.	Evaluation during lab class	Every week (total 10 weeks)	15 mins	20
2.	Record work	To be submitted every next week after completion of experiment	-	10
3.	Quiz	One week prior to end semester	1 hour	30
4.	Term Project	One week prior to end semester	-	10
5.	End semester evaluation	-	90 mins	30

Essential Readings: Text books, Reference books, website addresses and journals

1. John F.Wakerly, Digital Design, Fourth Edition, Pearson/PHI, 2006
2. John.M Yarbrough, Digital Logic Applications and Design, Thomson Learning, 2002.
3. Charles H.Roth. Fundamentals of Logic Design, Thomson Learning, 2003.
4. Donald P.Leach and Albert Paul Malvino, Digital Principles and Applications, 6th Edition, TMH, 2003.
5. Charles H. Roth, Jr., Lizy Kurian John Digital Systems Design Using VHDL, 2nd Edition, PWS Publishers, 1998.
6. Thomas L. Floyd, Digital Fundamentals, 8th Edition, Pearson Education Inc, New Delhi, 2003
7. Donald D.Givone, Digital Principles and Design, TMH, 2003
8. M. M. Mano, "Digital Design", 3rd ed., Pearson Education, Delhi, 2003.
9. Samir Palnitkar," Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Ed, Pearson Education Inc, New Delhi, 2001

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students through MIS and class committee meetings.

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/phone etc)

All the students are advised to check their NITT WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be intimated in Class Only.

ATTENDANCE

- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**
- Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

ASSESSMENT POLICY

1. Attending all the assessments is MANDATORY for every student.
2. If any student is not able to attend any of the Continuous Assessments due to genuine reason, student is permitted to attend the **compensation assessment*** (CPA) with Corresponding weightage. (This is not valid for students who have attendance lag also.)
3. Please refer institute B.Tech Regulations/guidelines for grading policy.

ACADEMIC HONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, CC-chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programme.

ADDITIONAL INFORMATION

Queries may also be emailed to the Course Coordinator directly at thavasi@nitt.edu

FOR APPROVAL

Course Faculty 30/7/19 (G. Thavasi Raja) **CC-Chairperson** 31/7/19 **HOD**