DEPARTMENT OF Electronics and Communication Engineering

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	B.Tech (ECE)		
Course Title	VLSI SYSTEMS		
Course Code	ECPC26	No. of Credits	03
Course Code of Pre-requisite subject(s)	Nil		
Session	Jan 2019	Section (if, applicable)	Both A & B
Name of Faculty	Dr. B Venkataramani	Department	ECE
Email	bvenki@nitt.edu bvenkii@gmail.com	Telephone No.	7708977953 0431 2503303
Name of Course Coordinator(s) (if, applicable)	Nil		
E-mail	NA	Telephone No.	NA
Course Type	☑ Core course	☐ Elective course	

Syllabus (approved in BoS)

VLSI design methodology, VLSI technology- NMOS, CMOS and BICMOS circuit fabrication. Layout design rules. Stick diagram. Latch up.

Characteristics of MOS and CMOS switches. Implementation of logic circuits using MOS and CMOS technology, multiplexers and memory, MOS transistors, threshold voltage, MOS device design equations MOS models, small-signal AC analysis. CMOS inverters, propagation delay of inverters, Pseudo NMOS Dynamic CMOS logic circuits, power dissipation.

Programmable logic devices- antifuse, EPROM and SRAM techniques. Programmable logic cells Programmable inversion and expander logic. Computation of interconnect delay, Techniques for driving large off-chip capacitors, long lines, Computation of interconnect delays in FPGAs Implementation of PLDs EPROM, EEPROM, static and dynamic RAM in CMOS.

An overview of the features of advanced FPGAs, IP cores, Softcore processors, Various factors determining the cost of a VLSI, Comparison of ASICs, FPGAs , PDSPs and CBICs . Fault tolerant VLSI architectures

VLSI testing -need for testing, manufacturing test principles, design strategies for test, chip level and system level test techniques.

Text Books

1. *N. H. E. Weste, D.F. Harris, "CMOS VLSI design", (4/e), Pearson , 2015.*
2. *J. Smith, "Application Specific Integrated Circuits, Pearson", 2011.*
3. *M.M.Vai, "VLSI design", CRC Press, 2001.*

Reference Books

1. *Pucknell & Eshraghian, "Basic VLSI Design", PHI, (3/e), 2003.* 2. *Uyemura, "Introduction to VLSI Circuits and Systems", Wiley, 2002*
COURSE OBJECTIVES
To introduce various aspects of VLSI circuits and their design including testing.

COURSE OUTCOMES (CO)	
Course Outcomes	**Aligned Programme Outcomes (PO)**
1. Describe the techniques used for VLSI fabrication, design of CMOS logic circuits, switches and memory	**PO1, PO3, PO4, PO5**
2. Describe the techniques used the design of CMOS logic circuits, switches and memory in VLSI	**PO1, PO3, PO4, PO5**
3. Generalize the design techniques and analyze the characteristics of VLSI circuits such as area, speed and power dissipation	**PO1, PO2, PO3, PO4, PO5,PO7, PO12**
4. Explain and compare the architectures for FPGA, PAL and PLDs and evaluate their characteristics such as area, power dissipation and reliability	**PO1, PO2, PO3, PO4, PO5,PO7, PO12**
5. Describe the techniques for fault tolerant VLSI circuits, Explain and compare the techniques for chip level and board level testing	**PO1, PO2, PO3, PO4, PO5,PO7, PO12**

COURSE TEACHING AND LEARNING ACTIVITIES		
Week	**Topic**	**Mode of Delivery**
Week 1 **(3 Contact Hours)**	VLSI design methodology, VLSI technology- NMOS, CMOS and BICMOS circuit fabrication.	**Lecture** **C&T/ PPT or any suitable mode**
Week 2 **(3 Contact Hours)**	Layout design rules. Stick diagram. Latch up. Characteristics of MOS and CMOS switches.	
Week 3 **(3 Contact Hours)**	Implementation of logic circuits using MOS and CMOS technology, multiplexers and memory,	
Week 4 **(3 Contact Hours)**	MOS transistors, threshold voltage, MOS device design equations. MOS models, small-signal AC analysis.	
ASSESSMENT I - 10 Marks		**Quiz**

Week 5 **(3 Contact Hours)**	CMOS inverters, propagation delay of inverters, Pseudo NMOS, Dynamic CMOS logic circuits, power dissipation.	
Week 6	**ASSESSMENT II - 20 Mark**	**Descriptive/Numerical (Written)**
Week 7 **(3 Contact Hours)**	Programmable logic devices-antifuse, EPROM and SRAM techniques. Programmable logic Cells.	
Week 8 **(3 Contact Hours)**	Programmable inversion and expander logic. Computation of interconnect delay, Techniques for driving large off-chip capacitors, long lines,	**Lecture C&T/ PPT or any suitable mode**
Week 9 **(3 Contact Hours)**	Computation of interconnect delays in FPGAs Implementation of PLD,	
ASSESSMENT III - 10 Marks		**Quiz**
Week 10 **(3 Contact Hours)**	EPROM, EEPROM, static and dynamic RAM in CMOS.	**Lecture C&T/ PPT or any suitable mode**
Week 11 **(3 Contact Hours)**	An overview of the features of advanced FPGAs, IP cores, Soft-core processors	
Week 12 **(3 Contact Hours)**	Various factors determining the cost of a VLSI, Comparison of ASICs, FPGAs , PDSPs and CBICs .	
Week 13 **(3 Contact Hours)**	Fault tolerant VLSI architectures VLSI testing -need for testing	
Week 14 **(3 Contact Hours)**	**ASSESSMENT IV - 20 Marks**	**Descriptive/Numerical (Written)**
Week 15 **(3 Contact Hours)**	manufacturing test principles, design strategies for test, chip level and system level test techniques.	
(3 Contact Hours)	**END ASSESSMENT – 40 Marks**	**Descriptive/Numerical (Written)**

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment I (Quiz)	1st week Feb	60 Minutes	10
2	Assessment II	3rd Week Feb	60 Minutes	20
3	Assessment III (Quiz)	2nd Week of March	60 Minutes	10
4	Assessment IV	4th Week of March	60 Minutes	20
5	Compensation Assessment*	1st Week of April	60 Minutes	20
6	Final Assessment *	4th Week of April	180 Minutes	40

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students after the lectures are over

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)

Only email

COMPENSATION ASSESSMENT POLICY

Equal weightage for portions from both Assessment II & IV would be included for the compensation assessment

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**
- Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

  The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

Every student is expected to score a minimum of Peak/3 or class average/2 whichever is lower of the maximum mark of the class in the total assessment to pass the course. Otherwise the student would be declared fail and 'F' grade will be awarded.

FOR APPROVAL

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____

Guidelines:

a) The number of assessments for a course shall range from 4 to 6.

b) Every course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.

d) The passing minimum shall be as per the regulations.

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2018	2017	2016	2015	
35% or class average/2 whichever is greater.		Peak/3 or class average/2 whichever is lower		40%

e) **Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.**

f) **Absolute grading policy shall be incorporated if the number of students per course is less than 10.**

g) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.