DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	***M. Tech.*** **VLSI System**		
Course Title	***Low Power VLSI Circuits***		
Course Code	***EC668***	**No. of Credits**	***3 (Three)***
Course Code of Pre-requisite subject(s)	***EC651 Analog IC Design*** ***EC653 Basics of VLSI***		
Session	January 2019	**Section (if, applicable)**	*NA*
Name of Faculty	*Dr. M.Bhaskar*	**Department**	*ECE*
Email	*bhaskar@nitt.edu*	**Telephone No.**	*0431-2503310*
Name of Course Coordinator(s) (if, applicable)	*Nil*		
E-mail	---	**Telephone No.**	---
Course Type	☐ **Core course** ☑ **Elective course**		

Syllabus (approved in BoS)

Evolution of CMOS technology, CMOS fabrication process, shallow trench isolation, Lightly-doped drain, Buried channel. BiCMOS and SOI CMOS technologies, second order effects, Modeling of MOS devices, Threshold voltage, Body effect, Short channel and Narrow channel effects, Electron temperature, MOS capacitance.

CMOS inverters, Differential static logic circuits, Pass transistor Bi-CMOS, SOI CMOS, Low voltage and low power CMOS static logic circuit design techniques.

Basic concepts of dynamic logic circuits. Charge sharing, Noise and race problems, NORA, Zipper, Domino, Dynamic differential, BiCMOS, low voltage and low power dynamic logic techniques.

CMOS memory circuits, SRAM, DRAM, Bi-CMOS and Nonvolatile memory circuits.

Basics of clock gating and power gating, CMOS VLSI systems, Adder circuits, Multipliers and advanced structures – PLA, PLL, DLL and processing unit.

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

Text Books

1. *J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009*
2. *J.B.Kuo and J.H.Lou, "Low-voltage CMOS VLSI Circuits", Wiley, 1999.*

Reference Books

1. *Michael Keating etal. "Low Power Methodology Manual For System-on-Chip Design" Springer, 2008*
2. *A.Bellaowar and M.I.Elmasry,"Low power Digital VLSI Design, Circuits and Systems", Kluwer, 1996.*

COURSE OBJECTIVES

To expose the students to the low voltage device modeling, low voltage, low power VLSI CMOS circuit and system design

COURSE OUTCOMES (CO)	
Course Outcomes	**Aligned Programme Outcomes (PO)**
1. *Acquire the knowledge about various CMOS fabrication process and its modelling. Infer about the second order effects of MOS transistor characteristics.*	**PO1,PO2,PO3**
2. *Analyze and implement various CMOS low voltage and low power static logic circuits.*	**PO1,PO2,PO3,PO4, PO5,PO7,PO8**
3. *Learn the design of various CMOS low voltage and low power dynamic logic circuits.*	**PO1,PO2,PO3,PO4, PO5,PO7,PO8**
4. *Learn the different types of memory circuits and their design.*	**PO1,PO2,PO3,PO4, PO5,PO7,PO8**
5. *Design and implementation of various structures for low power applications.*	**PO1,PO2,PO3,PO4, PO5,PO7,PO8**

COURSE PLAN – PART II

COURSE OVERVIEW

To give exposure CMOS device fabircation and its low voltage device modeling. Design of low voltage and low power static, dynamic VLSI circuits and memory circuits. Design of low power VLSI computational circuits.

COURSE TEACHING AND LEARNING ACTIVITIES

Sl. No.	Week	Topic	Mode of Delivery
1	1st week (3 contact hours)	Evolution of CMOS Technology, CMOS fabrication process. Low voltage issues.	PPT, Chalk and talk
2	2nd week (3 contact hours)	STI, LDD and buried channel effects Bi-CMOS fabrication, SOI-CMOS fabrication	PPT, Chalk and talk
3	3rd week (3 contact hours)	Second order effects of CMOS devices. Short channel, narrow channel, hot carrier effects	PPT, Chalk and talk
4	4th week (3 contact hours)	CMOS static circuit design, Differential circuit design	PPT, Chalk and talk
5	5th week (3 contact hours)	Bi-CMOS static circuit design, SOI CMOS static circuit design	PPT, Chalk and talk
6	6th week (3 contact hours)	Low power, low voltage circuit techniques. Basics of dynamic logic circuit design	PPT, Chalk and talk
7	7th week (3 contact hours)	Disadvantages of dynamic logic circuits and solutions	PPT, Chalk and talk
8	8th week (3 contact hours)	Dynamic differential logic circuit design	PPT, Chalk and talk
9	9th week (3 contact hours)	Bi-CMOS dynamic logic circuit design	PPT, Chalk and talk
10	10th week (3 contact hours)	Low voltage dynamic logic circuit design techniques	PPT, Chalk and talk
11	11th week (3 contact hours)	Memories basic concepts CMOS circuits for various blocks of SRAM	PPT, Chalk and talk
12	12th week (3 contact hours)	DRAM and SOI memory	PPT, Chalk and talk

COURSE ASSESSMENT METHODS (shall range from 4 to 6)				
Sl. No.	**Mode of Assessment**	**Week/Date**	**Duration**	**% Weightage**
1	Assessment - 1 (Descriptive exam) (1st and 2nd units)	5th week	1 hour	20 Marks
2	Assessment - 2 (Descriptive exam) (3rd and 4th units)	10th week	1 hour	20 Marks
3	Assignment (5th unit)	11th week	One week	10 Marks
CPA	Compensation Assessment (Descriptive exam) (1st to 4th units)	12th week	1 hour	20 Marks
4	Final Assessment (Descriptive exam) (All units – End semester)	3rd week of April	3 hours	50 Marks

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. *Feedback from students during class committee meetings*
2. *Feedback through MIS at the end of the semester*

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

COURSE ASSESSMENT:

1 *Attending all the assessments are MANDATORY for every student*
2 *If any of the student is not able to attend any of the continuous assessment descriptive examination due to genuine reason (any academic related work through department or medical grounds only), student is permitted to attend CPA.*
3 *Submission of assignments is MANDATORY for every student within the stipulated time failing which 10% weightage will not be considered for final grade assessment*
4 *There will not be any improvement test for the students who score low marks in continuous assessment test.*
5 *Finally, every student is expected to score minimum marks as per the regulations of the institute out of the total assessments 1,2,3,4/CPA and 5 to pass the course. Otherwise the student will be declared fail and 'F' grade will be awarded. Further the student can take up only FORMATIVE ASSESSMENT.*

MODE OF CORRESPONDENCE (email/ phone etc)

1 *All students are advised to check their NITT webmail regularly. All the details about the schedule of classes, schedule of assessments, course material and any other information regarding the course will be sent through webmail only.*
2 *Doubts regarding the course can be clarified by fixing proper timing with the teacher during working hours only.*
3 *Queries, if any regarding the course shall only through email to the teacher.*

COMPENSATION ASSESSMENT POLICY

1 *Any student who fails to maintain 75% attendance only on reasonable medical/official grounds needs to appear for the compensation assessment (CPA) classes.*
2 *The portion for compensation assessment will be the portion of assessment 1 and 2.*

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

1. *At least 75% attendance in each course is mandatory.*
2. *A maximum of 10% shall be allowed under On Duty (OD) category.*
3. *Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.*

ACADEMIC DISHONESTY & PLAGIARISM

1. *Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.*
2. *Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.*
3. *The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.*

The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

The faculty is available for consultation at times as per the intimation given by the faculty.

FOR APPROVAL

25/11/2019

Course Faculty _____ (M. BHASKAR)

CC-Chairperson _____ **HOD** _____

Guidelines:

a) The number of assessments for a course shall range from 4 to 6.

b) Every course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) **One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.**

d) The passing minimum shall be as per the regulations.

B.Tech. Admitted in				P.G.
2018	2017	2016	2015	
35% or class average/2 whichever is greater.		Peak/3 or class average/2 whichever is lower		40%

e) Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

f) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

g) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.