DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	HIGH SPEED SYSTEM DESIGN		
Course Code	EC679	No. of Credits	03
Course Code of Pre-requisite subject(s)	--		
Session	January 2019	Section (if, applicable)	NA
Name of Faculty	Ms.P.Muthu Krishnammal	Department	M.Tech(VLSI Systems)
Email	muthup@nitt.edu	Telephone No.	9884588247
Name of Course Coordinator	NA		
E-mail	--	Telephone No.	--
Course Type	PE		

Syllabus (approved in BoS)

- Functions of an Electronic Package, Packaging Hierarchy, IC packaging requirements and properties; materials and substrates; Interconnect Capacitance, Resistance and Inductance fundamentals;; IC assembly: , Wire bonding, Tape Automated Bonding, Flip Chip, wafer level packaging; impact on reliability and testability.
  Overview of Transmission line theory, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI; crosstalk and non-ideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise;
- Practical aspects of measurement at high frequencies; high speed oscilloscopes and logic analyzers
- Printed Circuit Board: Anatomy, CAD tools for PCB design, Standard fabrication, Micro via Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation cooling requirements.
- Reliability, Basic concepts, Environmental interactions. Thermal mismatch and fatigue failures thermo mechanically induced electrically induced chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.

COURSE OBJECTIVES

1. To apply the transmission line theory for the design and analysis of the charecteristics of interconnects in PCBs and VLSI chips
2. To introduce the different parameters which control the reliabilty of the PCBs and VLSI chips
3. To use test instruments to analyse the performance of high speed circuits
4. To introduce the techniques adopted for clock distribution and power distribution for high speed circuits
5. To study the characteristics of different types of materials used for packaging and PCB and their effect on the performance

COURSE OUTCOMES (CO)

CO1: Design of PCBs which minimize the EMI and operate at higher frequency.

CO2: Enable design of packages which can withstand higher temperature, vibrations and shock.

COURSE OUTCOMES	**Aligned Programme Outcomes (PO)**
1. Design of PCBs which minimize the EMI and operate at higher frequency.	**P1,P2,P4**
2. Enable design of packages which can withstand higher temperature, vibrations and shock.	**P6, P7,P11,P12**

COURSE PLAN – PART II

COURSE OVERVIEW

This course gives the procedure for the design as well as analysis of high speed printed circuit boards and very large scale integrated circuits. It also presents the details on different types of packages and their effect on the performance of the ICs. It provides the details on different types of noise and interference in the PCBs and the technique to be adopted to overcome them. The details of thermal management and their effect on reliability of the circuits are also provided.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	**Week/Contact Hours**	**Topic**	**Mode of Delivery**
1.	Week 1 **(3 Contact Hours)**	Functions of an Electronic Package, Packaging Hierarchy, IC packaging: MEMS packaging, consumer electronics packaging, medical electronics packaging, Trends, Challenges, Driving Forces on Packaging Technology, Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging, Material for high density interconnect substrates	**Lecture** **C&T/ PPT or any suitable mode**

2.	Week 2 **(3 Contact Hours)**	Overview of Transmission line theory, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI; crosstalk and non-ideal effects; signal integrity	**Lecture** **C&T/ PPT or any suitable mode**
3.	Week 3 **(3 Contact Hours)**	Impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise.	**Lecture** **C&T/ PPT or any suitable mode**
	ASSESSMENT I - 5 Marks		
4.	Week 4 **(3 Contact Hours)**	Electrical Anatomy of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference, Design Process Electrical Design: Interconnect Capacitance, Resistance and Inductance fundamentals; Transmission Lines	**Lecture** **C&T/ PPT or any suitable mode**
5.	Week 5	**ASSESSMENT II - 20 Marks**	**Descriptive / Numerical (Written)**
6.	Week 6 **(3 Contact Hours)**	Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI, Digital and RF Issues. Processing Technologies, Thin Film deposition, Patterning, Metal to Metal joining.	**Lecture** **C&T/ PPT or any suitable mode**
7.	Week 7 **(3 Contact Hours)**	IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding	**Lecture** **C&T/ PPT or any suitable mode**
8.	Week 8 **(3 Contact Hours)**	Flip Chip, Wafer Level Packaging, reliability, wafer level burn – in and test- Single chip packaging: functions, types, materials processes, properties, characteristics, trends. Multi chip packaging types, design, comparison, trends. Passives: discrete, integrated, embedded – encapsulation and sealing: fundamentals, requirements, materials, processes.	**Lecture** **C&T/ PPT or any suitable mode**

	ASSESSMENT III - 5 Marks		
9.	Week 9	**ASSESSMENT II - 20 Marks**	**Descriptive / Numerical (Written)**
10.	Week 10 **(3 Contact Hours)**	Printed Circuit Board: Anatomy, CAD tools for PCB design, Standard fabrication, Micro via Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges.	**Lecture C&T/ PPT or any suitable mode**
11.	Week 11 **(3 Contact Hours)**	Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation – Cooling requirements.	**Lecture C&T/ PPT or any suitable mode**
12.	Week 12 **(3 Contact Hours)**	Reliability, Basic concepts, Environmental interactions. Thermal mismatch and fatigue – failures – thermo mechanically induced – electrically induced – chemically induced.	**C&T/ PPT or any suitable mode**
13.	Week 13 **(3 Contact Hours)**	Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.	**Lecture C&T/ PPT or any suitable mode**

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment I	1st week Feb		5
2	Assessment II (CT I)	3rd Week Feb	60 Minutes	20
3	Assessment III	2nd Week of March		5
4	Assessment IV (CT II)	4th Week of March	60 Minutes	20
5	Assessment V (CPA)	1st Week of April	60 Minutes	20
6	End Assessment	4th Week of April	180 Minutes	50

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

CORRESPONDENCE

1. All the students are advised to check their NITT WEBMAIL/group mail/suggested by the course faculty, class representative regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through them only.
2. Queries (if required) to the course teacher shall only be emailed to the email id specified by the teacher.

ATTENDANCE

3. Attendance will be taken by the faculty in all the contact hours. Every student should try to be present in the class during these contact hours.
4. Those students who missed any of the continuous assessments (CAs) due to genuine reasons can appear for retest. The scores in the retest will be taken into account for computing marks for CA.

ASSESSMENT

5. Attending all the assessments are MANDATORY for every student.
6. Every student is expected to score minimum 40% of the maximum mark of the class in the total assessment (1, 2, 3, 4 and 6) to pass the course. Otherwise the student would be declared fail and 'F' grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.

ACADEMIC HONESTY & PLAGIARISM

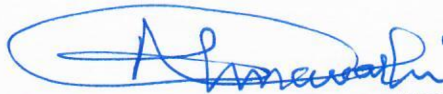
1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any Assessments is considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL INFORMATION

FOR APPROVAL

Course Faculty ____________

[Ms. P. MUTHU KRISHNAMMAL]



CC-Chairperson ____________

HOD ____________