DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	MASTER OF TECHNOLOGY VLSI SYSTEM		
Course Title	VLSI SYSTEM TESTING		
Course Code	EC652	No. of Credits	3
Course Code of Pre-requisite subject(s)	EC653 Basics of VLSI		
Session	January 2019	Section (if, applicable)	
Name of Faculty	R.THILAGAVATHY	Department	ECE
Email	thilagavathy@nitt.edu	Telephone No.	0431-2503313
Name of Course Coordinator(s) (if, applicable)			
E-mail		Telephone No.	
Course Type	[√] Core course	[ ] Elective course	

Syllabus (approved in BoS)

Basics of Testing: Fault models, Combinational logic and fault simulation, Test generation for Combinational Circuits. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation.

Universal test sets: Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

CMOS testing: Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.

Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.

Built-in self-test: Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Text Books:

- Jha & S.D. Gupta, "Testing of Digital Systems", Cambridge, 2003.
- 2. W. W. Wen, "VLSI Test Principles and Architectures Design for Testability", Morgan Kaufmann Publishers. 2006.

Reference Books:

- Michael L. Bushnell &Vishwani D. Agrawal," Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits", Kluwar Academic Publishers. 2000.
- P. K. Lala," Digital circuit Testing and Testability", Academic Press. 1997.
- M. Abramovici, M. A. Breuer, and A.D. Friedman, "Digital System Testing and Testable Design", Computer Science Press, 1990.

COURSE OBJECTIVES

To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned Programme Outcomes (PO)**
After successful completion of the course the students are able to	
CO1: Analyse the concepts in testing which can help them design a better yield in IC design.	PO1,PO2,PO3-H PO4,PO5-M PO9-L
CO2: Tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.	PO1,PO2,PO3,PO5,PO7-H PO4,PO9-M
CO3: Describe the various test generation methods for static & dynamic CMOS circuits.	PO2-H PO1,PO5-M PO3,PO4PO9-L
CO4: Explain the design for testability methods for combinational & sequential CMOS circuits.	PO2,PO5-H PO4-M PO1,PO3PO9-L
CO5: Synthesize the BIST techniques for improving testability.	PO2,PO4,PO5-H PO3-M PO1,PO7,PO9-L
	H-High M- Medium L-Low

COURSE PLAN – PART II

COURSE OVERVIEW

This course will Introduce fundamental concepts and various aspects of VLSI testing and Focus on Importance of testing in the design and manufacturing processes. This course will explore Challenges in test generation and fault modeling, Levels of abstraction in VLSI testing. This course may provide overview of VLSI test technology. Students will acquire the knowledge about the following topics:

- Test process and ATE
- Test Economics
- Fault Models
- Fault Simulation
- Testability Measures
- ATPG
- Different Testing Methods (IDDQ, Delay etc.)
- Scan design
- BIST (Built in Self Test)
- Boundary Scan ,Memory test
- Other advanced topics

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1.	First week of January	Introduction to basic testing principles. Analysis of faults, Test economics, Fault models	PPT
2.	Second week of January	Combinational circuit ATPG testing, Sensitized path based testing, Logic simulation	Chalk & Talk PPT
3.	Third week of January	Testability measures (SCOAP), Direct and Indirect Implications, D-Algorithm and PODEM algorithm	Chalk & Talk
4.	Fourth week of January	Fault Collapsing and dropping, Serial and parallel fault simulation, Deductive fault simulation, IDDQ testing	PPT
5.	First week of February	Sequential ATPG and delayed reconvergence, State table method and self-hiding, Extended D - Algorithm	Chalk & Talk PPT
6.	Second week of February	Universal test sets, Pseudo –exhaustive testing, Clocking schemes for delay fault testing	Chalk & Talk PPT
7.	Fourth week of February	Testability classification for Path delay fault, Test generation for Gate delay fault and segment, delay fault	Chalk & Talk PPT
8.	First week of March	Testing dynamic domino circuits, Testing of DCVS circuits, Testing of CMOS static circuits	Chalk & Talk PPT
9.	Second week of March	Check points and check point transistors, Testing using tree representation	Chalk & Talk PPT
10.	Third week of March	Introduction to fault diagnosis, Cause – effect diagnosis, Effect – cause diagnosis	Chalk & Talk PPT
11.	First week of April	Scan design testability, Scan cell design for DFT, Scan design flow	Students seminar using PPT
12.	Second week of April	Scan design verification test and cost, Built in self-test (BIST) Architecture	Students seminar using PPT
13.	Third week of April	BIST design rules, LFSR, CA, Signature Analysis, Fault coverage Enhancement	Students seminar using PPT
14.	Fourth week of April	Memory test	Students seminar using PPT

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Assessment -1 Written test (Descriptive type)	Third week of February	1 Hour	20 marks (1 ½ units)
2.	Assessment -2 Written test (Descriptive type)	Fourth week of March	1 Hour	20 marks (1 ½ units)
3.	Assessment - 3 Seminar (oral presentation)	April (Four weeks)	30 minutes(per student)	10 marks (2 units) Unit 4 & 5
CPA	Compensation Assessment*	April first week (If applicable)	1 Hour	20 marks (3 units)

				Unit 1,2 & 3
4.	Final Assessment *	May first week	3 Hours	50 marks (All 5 units)

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Course feedback is assessed through

1. Class committee meeting
2. Frequently ask the questions in the class and analyzes the responses
3. Course exit survey form

Course Attainment is calculated through

Direct tools (Exams and Assignments)

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)

Information regarding this course will be intimated in class/ over phone/ in faculty room / through their webmail.

COMPENSATION ASSESSMENT POLICY

1. Any student who fails to maintain 75% attendance only on reasonable medical grounds needs to appear for the compensation assessment (CPA) classes. On successful completion of CPA classes along with assessment criteria will be eligible for attending the end semester examination.
2. If any of the student is not able to attend Assessment -1 and Assessment- 2 examinations due to genuine reason (any academic related work through department or medical grounds only), may appear for compensation assessment (CPA) which will carry 20% weight. CPA cannot be considered as an improvement exam.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**
- Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

  The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

Any queries send a mail to thilagavathy@nitt.edu

FOR APPROVAL

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____

Guidelines:

a) The number of assessments for a course shall range from 4 to 6.

b) Every course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered. Details of compensation assessment to be specified by faculty.

d) The passing minimum shall be as per the regulations.

B.Tech. Admitted in				P.G.
2018	2017	2016	2015	
35% or class average/2 whichever is greater.		Peak/3 or class average/2 whichever is lower		40%