#### NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

Course Title	ANALOG IC Design		
Course Code	ECHO19	No. of Credits	03
Department	Electronics and Communication Engineering	Faculty	Dr. B Venkataramani
Pre-requisites Course Code	- Propertion		les (viirot) viii in 1918
Course Coordinator	-		
Other Course Teacher(s)/Tutor(s) E-mail	Telephone No.  bvenki@nitt.edu 7708977953 0431 2503303		
Course Type	Program Core/ Honours elective		

#### **COURSE OVERVIEW**

This course develops the expertise to draw the equivalent circuits for single stage and multistage amplifiers using MOS. The effect of different types of loads on the performance is studied. The evaluation of the frequency response of the circuits and the application of different types of feedback on MOS amplifiers are studied. The different sources of noise in MOS circuits and computation of noise in MOS amplifiers is studied. The implementation of switched capacitor circuits, current mirrors and bandgap reference are also introduced

#### **COURSE OBJECTIVES**

To develop the expertise for designing and analysing the MOS analog VLSI circuits including single stage and multistage amplifiers with and without feedback and with different types of loads

#### COURSE OUTCOMES (CO)-

Students are able to

- CO1: To design single stage MOS amplifiers and analyse its performance
- CO2: To design and understand the operation of differential amplifiers, Compute the common mode and differential gain, and evaluate the effect of mismatches and different loads
- CO3: Study and implementation of two stage MOS operational amplifiers and techniques for gain enhancement and common mode feedback
- CO4: Study and understand switched capacitor based circuits, their imperfections and remedies. Study and realise bandgap reference circuits, current mirrors
- CO5: Study and analyse the frequency response of MOS amplifiers and the effect of feedback on MOS amplifiers. : Study and analyse the noise in single stage and multistage amplifiers

S.No.	Week	Topic	Mode of Delivery
1.	1-3 AUG 2018	Why Analog? Basic MOS Device	Lecture
	Week 1	Physics – MOS I/V Characteristics,	C&T/ PPT or any suitable
	(3 Contact Hours)	Second Order effects,	mode

2.	Week 2 & 3 (3 Contact Hours)	MOS Device models Single Stage Amplifiers – Basic Concepts, Common Source Stage with different loads	Silin mal/selectoreus	
3.	Week 4 (3 Contact Hours)	Source Follower, Common Gate Stage, Cascode Stage.	Course Consultation	
	ASSESSMENT I - 10 Marks		Quiz	
4.	Week 5 (3 Contact Hours)	Differential Amplifiers – Single Ended and Differential Operation, Basic Differential Pair,	en e	
5.	5-7 SEP Week 6 (3 Contact Hours)	Common-Mode Response, Differential Pair with MOS loads, Gilbert Cell.	Lecture C&T/ PPT or any suitable mode	
6.	Week 6 (3 Contact Hours) 12-14 SEP	Passive and Active Current Mirrors  - Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Frequency Response of Amplifiers - General Considerations, Common Source Stage,	mode	
	Week 7	ASSESSMENT II - 20 Mark	Descriptive/Numerical (Written)	
7.	Week 8 (3 Contact Hours) SEP 26-28	Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair.	Lecture	
8.	Week 9 (3 Contact Hours) 3-5 OCT	Feedback Amplifiers – General Considerations,	C&T/ PPT or any suitable mode	
9.	Week 10 (3 Contact Hours) 10-12 OCT	Feedback Topologies, Effect of Loading	nidus burning (199. ) =	
ADDI	ASSES	SSMENT III - 10 Marks	Quiz	
10.	Week 11 (3 Contact Hours)	Introduction to switched capacitor circuits, MOS Switches, Speed Considerations, Precision Considerations, Nonidealities of MOS switches, Charge injection	DINA CONHORST SERUGO SHOW ARE DINE DORKED	
11.	Week 12 (3 Contact Hours)	cancellation  Switched Capacitor amplifiers, Unity gain buffer- speed and precision considerations, Non inverting amplifier-speed and	Lecture C&T/ PPT or any suitable mode	

		precision considerations	
12.	Week 13 (3 Contact Hours)	Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps,	d DV ROSCHEDBROG
lo el Degar	Week 14	ASSESSMENT IV - 20 Marks	Descriptive/Numerical (Written)
13.	Week 15 (3 Contact Hours)	Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation.	Lecture C&T/ PPT or any suitable mode
14.	Week 16 (3 Contact Hours)	Bandgap References, Nonlinearity and Mismatch	Lagine dea encera Lagine unituación
15.	Week 17 (3 Contact Hours)	Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.	
16.	(3 Contact Hours)	END ASSESSMENT – 40 Marks	Descriptive/Numerical (Written)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Assessment I (Quiz)	3 <sup>rd</sup> Week of August	60 Minutes	10
2.	Assessment II	3 <sup>rd</sup> Week of September	60 Minutes	20
3.	Assessment III (Quiz)	1st Week of October	60 Minutes	10
4.	Assessment IV	1st Week of November	60 Minutes	20
5.	Assessment V (CPA)	3 <sup>rd</sup> Week of November	60 Minutes	20
6.	End Assessment	1st Week of December	180 Minutes	40

# ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc Text Books

Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Edition 2002.

David A. Johns and Ken Martin, Analog Integrated Circuit Design, Wiley, 1997.
R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, Wiley, (3/e), 2010.
Philip.E.Allen, et al. CMOS Analog Circuit Design, Oxford University Press, 2002.
Paul. R.Gray, et al. Analysis and Design of Analog Integrated Circuits, Wiley, (4/e), 2001.

# COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

Feedback from the students during class committee meetings Anonymous feedback through questionnaire

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

### CORRESPONDENCE

1. All the students are advised to check their NITT WEBMAIL/group mail/suggested by the course faculty, class representative regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through them only.

2. Queries (if required) to the course teacher shall only be emailed to the email id specified

by the teacher.

## **ATTENDANCE**

3. Attendance will be taken by the faculty in all the contact hours. Every student should try to be present in the class during these contact hours.

4. Those students who missed any of the continuous assessments (CAs) due to genuine reasons can appear for retest. The scores in the retest will be taken into account for computing marks for CA.

### **ASSESSMENT**

5. Attending all the assessments are MANDATORY for every student.

6. Every student is expected to score minimum 40% of the maximum mark of the class in the total assessment (1, 2, 3, 4 and 6) to pass the course. Otherwise the student would be declared fail and 'F' grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.

# ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any assessments is considered dishonest.

2. Tendering of information such as giving one's program, simulation work, assignments to

another student to use or copy is also considered dishonest.

3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.

4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.

5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

## ADDITIONAL COURSE INFORMATION

FOR	SENATE'S	CONSIDERATION

Course Faculty

CC-Chairperson M.N.