DEPARTMENT OF Electronics & Communication Engineering

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	**B.Tech., Electronics & Communication Engineering**		
Course Title	Digital System Design		
Course Code	**EC661**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**-**	**-**	**-**
Session	**July, 2018**	**Section (if, applicable)**	**-**
Name of Faculty	**Dr. Menka**	**Department**	**ECE**
Email	**menka@nitt.edu**	**Telephone No.**	**+91-9416794011**
Name of Course Coordinator(s) (if, applicable)	**Dr. Menka**		
E-mail		**Telephone No.**	
Course Type	☐ **Core course**	☑ **Elective course**	

Syllabus (approved in BoS)

UNIT 1. Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.

UNIT 2. Combinational network delay. Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis.

UNIT 3. Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.

UNIT 4. Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.

UNIT 5. Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures-Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.Text Books

Text books-

1. Computer Architecture: A Constructive Approach, Arvind, Rishiyur S. Nikhil, Joel S. Emer, and Murali Vijayaraghavan *(Revision: August 25, 2015)* (Available online: http://csg.csail.mit.edu/6.375/6_375_2016_www/resources/archbook_2015-08-25.pdf)

2. Moris Mano, , 4th Edition https://docs.google.com/file/d/0B8-drkZsESDnN2NmYTQxYjQtYTMwZi00N2IzLTkxNjgtZjI1NTZiN2FjNDli/edit
3. N.H.E.Weste, D. Harris, *"CMOS VLSI Design", Pearson, latest edition*
4. W. Wolf, "FPGA based system Design", Pearson 2004
5. *S. Hauck, A. DeHon, "*Reconfigurable computing: the theory and practice of FPGA-based*", Elsevier 2008*

Reference Books

6. Recent literature in Digital System Design.
7. *John Wakerly, "Digital Design Principles" Prentic Hall* *https://profs.basu.ac.ir/abbasi/upload_file/932.2374.file_ref.2588.3001.pdf*
8. C.Roth, "Fundamentals of Digital Logic Design", Jaico Publishers 2009
9. C. Bobda, 'Introduction to reconfigurable computing', Springer, 2007

Websites/Online Materials

10. *http://csg.csail.mit.edu/6.375/6_375_2016_www/handouts.html*
11. *http://www.cs.columbia.edu/~nowick/nowick-singh-ieee-dt-11-published.pdf*
12. *Other material will be shared time to time via mail*

COURSE OBJECTIVES

- To make the students understand the fundamentals of complex digital system design.
- To train them to apply these to real life project
- To train through experiential learning

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned Programme Outcomes (PO)**
To make the students understand the fundamentals of complex digital system design. To train them to apply these to real life project To train through experiential learning	

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned Programme Outcomes (PO)**
CO1: To describe the concept of Digital system Design CO2: To describe the Synchronous and Asynchronous machines CO3: Describe effect of timing and power issues on digital systems	PO1: Understand of Digital system Design. PO2: Apply the basic concept to higher order complex digital systems. PO3: Analyze a given circuit using basic concepts of Digital system analysis

CO4: Illustration of different combinational & Sequential circuits CO5: Reconfigurable computing	PO4: To understand how to apply the knowledge to Synthesize and find out time and power issues in complex systems

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1.	1, 2 slots	Introduction to the course, current market share and opportunities in digital system design field across the globe	C&T, PPT, group discussion, peer learning, experiential learning (out of class), any suitable model
2.	2, 3 slots	Basic combinational and sequential circuits, Introduction to FSM	
3.	3, 3 slots	Moore and Mealy FSM with example, synthesis of digital systems, Hazards	
4.	4, 3 slots	Analysis of digital systems, RTL Design with GCD example	
5.	5, 3 slots	Digital lock design example, asynchronous digital system design, state minimization –implication table, state equivalence	
6	6, 2 slots	Dynamic and Static timing analysis - Critical path analysis	
7	7, 3 slots	Power and energy optimisation	
8	8, 3 slots	Rules for clocking performance analysis	
9	9, 3 slots	Sequencing static & dynamic circuits, Synchronisers	
10	10, 2 slots	Datapath and array subsystems- addition subtraction, comparator	
11	11, 3 slots	..counter, coding, multiplication, division	
12	12, 3 slots	Memories and their working-SRAM, DRAM, ROM, serial access memory, context addressable memory	
13	13, 3 slots	Reconfigurable computing- fin grain, coarse grain architectures, pipeline reconfigurable, parallel processing	
14	14, 3 slots	Revision	

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	I (Close book)	1st week Oct. '18	60 Minutes	20
2	II (Close book)	2nd Week of Nov. ' 18	60 Minutes	20
3	III (Open book)	4th week of Oct.'18 (Experiential)	NA	10
CPA	Compensation Assessment*			
4	IV (Open book)	3rd week of Nov.' 18	NA	10
5	Final Assessment *	2nd Week of Nov ' 18	180 Minutes	40

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings.

Anonymous feedback through questionnaire.

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)

1. All the students are advised to check their mail Ids regularly. All the correspondence

(schedule of classes/ schedule of assessment/ course material/ any other information

Regarding this course) will be intimated in Class or mail.

COMPENSATION ASSESSMENT POLICY

a. Compensation exam can only be conducted if the reason is genuine, e.g. unavoidable medical emergency.
b. The candidates are requested to intimate well in time and they need to produce proof for the same
c. The application should come through HoD/Class Chairperson

- A maximum of 10% shall be allowed under On Duty (OD) Category.
- Students with lesser than 65% attendance will be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY AND PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero marks to be awarded for thr offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programs.

ADDITIONAL INFORMATION

FOR APPROVAL

3/10/18

Course faculty – Dr. Menka

3.10.2018

CC-Chairperson- Dr.P.Muthuchidambaranathan

HoD- Dr.G.Lakshmi Narayanan

Guidelines:

a. The number of assessments for a course shall range from 4 to 6.
b. Every course shall have a final assessment on the entire syllabus with at least 30% weightage.
c. One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered. Details of compensation assessment to be specified by faculty.
d. The passing minimum shall be as per the regulations.
e. Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.
f. Absolute grading policy shall be incorporated if the number of students per course is less than 10.
g. Necessary care shall be taken to ensure that the course plan is reasonable and is objective.