DEPARTMENT OF ECE

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	DIGITAL ELECTRONICS LABORATORY		
Course Code	ECLR 11	No. of Credits	1
Course Code of Pre-requisitesubject(s)	ECPC14	Faculty	Dr.R.Malmathanraj
Session	July 2018	Section (if, applicable)	B
Name of Faculty	Dr.R.Malmathanraj	Department	ECE
Email		Telephone No.	7639972187
Name of Course Coordinator(s) (if, applicable)			
E-mail		Telephone No.	
Course Type	* Core course	Elective course	

Syllabus (approved in BoS)

Study of logic gates and verification of Boolean Laws.
Design of adders and subtractors.
Design of code converters.
Design of Multiplexers.
Design of Demultiplexers.
Design of Encoder and Decoder.
2-bit and 8-bit magnitude comparators.
Study of flip-flops.
Design and implementation of counters using flip -flops.
Design and implementation of shift registers.

COURSE OBJECTIVES

To understand and analyse the basic concepts of Digital Circuit design.

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
1. To Design and implement the digital circuits	
2. To involve elegancy in the design of digital circuits	
3. To prepare the documentation and technical report of the work done in the lab.	

COURSE PLAN – PART II

COURSE OVERVIEW

The lab class is necessary for the students to have hands on training on what they learn in the Theory. Implementation of Digital circuits requires prerequiste knowledge about the concepts in Digital eletronics. The students will learn to implement combinational , sequential circuits in hardware and simulation.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	Week 1 (3 contact Hours)	Study of logic gates and verification of Boolean Laws.	Practical
2	Week 2 (3 contact Hours)	Design of adders and subtractors. Design of code converters.	Practical
3	Week 3 (3 contact Hours)	Design of Multiplexers. Design of De-multiplexers.	Practical
4	Week 4 (3 contact Hours)	Design of Encoder and Decoder	Practical
5	Week 5 (3 contact Hours)	2-bit and 8-bit magnitude comparators.	Practical
6	Week 6(3 contact Hours)	Study of flip-flops.	Practical
7	Week 7 (3 contact Hours)	Design and implementation of counters using flip -flops.	Practical
8	Week 8 (3 contact Hours)	Design and implementation of shift registers.	Practical
9	Week 9 (3 contact Hours)	Compensation Assessment	Practical
10	Week 10 (3 contact Hours)	Implementation of Combinational Circuits using Verilog	Simulation
11	Week 11 (3 contact Hours)	Implementation of sequential Circuits using Verilog	Simulation

12	Assessment II	Mini Project
13	Assessment III	Quiz (Written exam)
14	Assessment IV	Lab Exam

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	ASSESSMENT I (Continuous evaluation)	On Every lab class	3 hours in each lab class	40%
2	ASSESSMENT II* (Quiz (Written exam))	Date and Time will be announced later	50 minutes	25%
3	ASSESSMENT III* (Mini project)	Date and Time will be announced later		5%
4	Compensation Assessment	-	Refer course policy	
5	ASSESSMENT IV* (Lab Exam)	During I week of November.	120 minutes	30%

***mandatory; refer to guidelines on page 4**

Attending all the assessments are MANDATORY for every student.

ESSENTIAL READING

1. Textbooks mentioned in ECPC 14 Course plan.
2. Lab manual which will be given by the Faculty handling the lab.

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. Feedback from the students during the class committee meeting.
2. Queries through questionnaire.
3. Course attainment is calculated through Direct tools (Exams)

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

1. All the students are advised to come to class regularly. All the correspondence(Schedule of the classes/ Schedule of the assessment/Course material/any other information regarding this course) will be intimated in the class.
2. Queries (if required) to the course teacher shall be emailed to the email address specified.

ATTENDANCE

- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**

Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

COMPENSATION ASSESSMENT

1.Attending all the lab classes is compulsory for every student. However if due to genuine reasons he/she is unable to attend the lab class he may be permitted to do the experiment in the compensation lab class with prior permission.

ACADEMIC HONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

1. Attending all the assessments is mandatory for every student.
2. The passing minimum shall be as per the Office of the Dean (Academic) instructions. Hence, every student is expected to score the minimum mark to pass the course as prescribed by the Office of the Dean (Academic). Otherwise the student would be declared fail and 'F' grade will be awarded.

FOR APPROVAL

Course Faculty ________ CC-Chairperson ________ HOD ________

Dr. R. Malmathanraj.

Guidelines:

a) The number of assessments for a course shall range from 4 to 6.
b) **Every course shall have a final assessment on the entire syllabus with at least 30% weightage.**
c) **One compensation assessment for absentees in assessments (other than final assessment) is mandatory. This is not applicable for project work/industrial lectures/internship.**
d) The policy for attendance for the course should be clearly specified.
e) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.