DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	**DSP Architecture**		
Course Code	**EC 612**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**None**		
Session	**January - 2018**	**Section (if, applicable)**	**-**
Name of Faculty	**V.Thenmozhi**	**Department**	**M.TECH –VLSI SYSTEMS**
Email	**mozhi@nitt.edu**	**Telephone No.**	**-**
Name of Course Coordinator(s) (if, applicable)	**-**		
E-mail		**Telephone No.**	
Course Type	✓ **Elective course**	☐ **Core course**	

Syllabus (approved in BoS)

Fixed-point DSP architectures. TMS320C54X, ADSP21XX, SP56XX architecture details. Addressing modes. Control and repeat operations. Interrupts. Pipeline operation. Memory Map and Buses. TMS320C55X architecture and its comparison.
Floating-point DSP architectures. TMS320C67X, DSP96XX architectures. Cache architecture. Floating-point Data formats. On-chip peripherals. Memory Map and Buses.
On-chip peripherals and interfacing. Clock generator with PLL. Serial port. McBSP. Parallel port. DMA. EMIF. Serial interface-Audio codec. Sensors. A/D and D/A interfaces. Parallel interface-RAM and FPGA. RF transceiver interface. DSP tools and applications. Implementation of Filters, DFT, QPSK Modem, Speech processing. Video processing, Video Encoding / Decoding. Biometrics. Machine Vision.
High performance computing (HPC).Digital Media Processors. Video processing sub systems. Multi-core DSPs. OMAP. CORTEX, SHARC, SIMD, MIMD Architectures.

COURSE OBJECTIVES

To give an exposure to the various fixed point and floation point DSP architectures and to implement real time applications using these processors.

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
1. Learn the architecture details fixed and floating point DSPs.	PO1,PO8
2. Infer about the control instructions, interrupts, and pipeline operations, memory and buses.	PO2
3. Illustrate the features of on-chip peripheral devices and its interfacing with real time application devices.	PO7
4. Learn to implement the signal processing algorithms and applications in DSPs.	PO12
5. Learn the architecture of advanced DSPs.	PO6

COURSE PLAN – PART II			
COURSE OVERVIEW			
This course provides the knowledge about various DSP architectures, their addressing modes and data formats. Students will be able to learn about On-chip peripherals, memory mapping and bus architectures of various DSP processors. They can acquire knowledge about real time implementation of applications like speech processing, video processing, biometrics etc.,			
COURSE TEACHING AND LEARNING ACTIVITIES			
S.No.	**Week/Contact Hours**	**Topic**	**Mode of Delivery**
1	1st week of January (3 contact Hours)	Fixed-point DSP architectures. TMS320C54X, ADSP21XX	Chalk & Talk, PPT or any suitable mode
2	2nd week of January (3 contact Hours)	SP56XX architecture details. Addressing modes. Control and repeat operations. Interrupts	
3	3rd week of January (3 contact Hours)	Pipeline operation. Memory Map and Buses, TMS320C55X architecture and its comparison	
4	4th week of January (3 contact Hours)	Floating-point DSP architectures. TMS320C67X, DSP96XX architectures	
5	1st week of February (3 contact Hours)	Cache architecture. Floating-point Data formats. On-chip peripherals **First Assignment/quiz - 5marks**	
6	2nd week of February (3 contact Hours)	**First Assessment – 20 marks**	
7	3rd week of February (3 contact Hours)	Memory Map and Buses, On-chip peripherals and interfacing.	Chalk & Talk, PPT or any suitable mode
8	4th week of February (3 contact Hours)	Clock generator with PLL. Serial port, McBSP. Parallel port. DMA. EMIF	
9	1st week of March (3 contact Hours)	Serial interface-Audio codec. Sensors. A/D and D/A interfaces **Second Assignment/ quiz - 5marks**	
10	2nd week of March (3 contact Hours)	**Second Assessment- 20marks**	

11	3rd week of March (3 contact Hours)	Parallel interface-RAM and FPGA. RF transceiver interface	Chalk & Talk, PPT or any suitable mode
12	4th week of March (3 contact Hours)	DSP tools and applications. Implementation of Filters DFT, QPSK Modem,	
13	1st week of April (3 contact Hours)	Speech processing. Video processing, Video Encoding / Decoding Biometrics. Machine Vision.	
		Compensation Assessment-20marks	
14	2nd week of April (3 contact Hours)	High performance computing (HPC),Digital Media Processors. Video processing sub systems	Chalk & Talk, PPT or any suitable mode
15	3rd week of April (3 contact Hours)	. Multi-core DSPs OMAP. CORTEX, SHARC, SIMD, MIMD Architectures	
		Final Assessment-50marks	

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	First Assessment	2nd week of February	(60 minutes)	20 marks
2	Second Assessment	2nd week of March	(60 minutes)	20 marks
3	First Assignment	1st week February	(60 minutes)	05 marks
4	Second Assignment	1st Week of March	(60 minutes)	05 marks
CPA	Compensation Assessment*	1st Week of April	(60 minutes)	20 marks
6	Final Assessment *	4th Week of April	(180 minutes)	50 marks

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. Feedback from the students during class committee meeting.
2. Queries through questionnaire.

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

All the students are advised to come to class regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be intimated in class/ over phone/ in faculty room/ through their webmail.

ATTENDANCE

All the students should maintain minimum 75% of physical attendance in these contact hours to attend the end semester exam. However, the relaxation will be given for leave on medical, and other essential requirements followed in the institute. Those who have less than 75% attendance can take up only FORMATIVE ASSESSMENT

COMPENSATION ASSESSMENT

Attending all the assessments is mandatory. Students absenting from any assessment(s), on genuine reason, may appear for compensation assessment (CPA) which will carry 20% weight. CPA cannot be considered as an improvement exam or as compensation for attendance.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any assessments is considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.

ADDITIONAL INFORMATION

Queries and feedback may also be emailed to the Course Faculty at mozhi@nitt.edu

FOR APPROVAL

Course Faculty V. Thbi **CC-Chairperson** B Mahadevi **HOD**