DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I								
Course Title	COMPUTER ARCHITECTURE AND ORGANIZATION							
Course Code	ECPE24	No. of Credits	03					
Course Code of Pre- requisite subject(s)	None							
Session	Jan. 2018	Section (if, applicable)	A & B					
Name of Faculty	M.Gayathri Devi	Department	ECE					
Email	mgayathri@nitt.edu	Telephone No.	8148421338					
Name of Course								
Coordinator(s)	-							
(if, applicable)								
E-mail		Telephone No.						
Course Type	Core course	Core course Elective course						

Syllabus (approved in BoS)

Introduction: Function and structure of a computer, Functional components of a Computer, Interconnection of components, Performance of a computer.

Representation of Instructions: Machine instructions, Memory locations & Addresses, Operands, Addressing modes, Instruction formats, Instruction sets, Instruction set architectures - CISC and RISC architectures, Super scalar Architectures, Fixed point and floating point operations.

Basic Processing Unit: Fundamental concepts, ALU, Control unit, Multiple bus organization, Hardwired control, Micro programmed control, Pipelining, Data hazards, Instruction hazards, Influence on instruction sets, Data path and control considerations, Performance considerations.

Memory organization: Basic concepts, Semiconductor RAM memories, ROM, Speed - Size and cost, Memory Interfacing circuits, Cache memory, Improving cache performance, Memory management unit, Shared/Distributed Memory, Cache coherency in multiprocessor, Segmentation, Paging, Concept of virtual memory, Address translation, Secondary Storage devices.

I/O Organization: Accessing I/O devices, Input/output programming, Interrupts, Exception Handling, DMA, Buses, I/O interfaces- Serial port, Parallel port, PCI bus, SCSI bus, USB bus, Firewall and Infini band, I/O peripherals.

TextBooks

- 1. C.Hamacher Z. Vranesic and S. Zaky, "Computer Organization", McGraw-Hill,2002.
- 2. W. Stallings, "Computer Organization and Architecture Designing for Performance". Prentice Hall of India. 2002.
- 3. B, Parhami, "Computer Architecture, From Microprocessors to Supercomputers," Oxford University Press, Reprint2014.

ReferencesBooks

- 1. D. A. Patterson and J. L. Hennessy, "Computer Organization and Design,
- 2. Morgan Kaufmann,"The Hardware/Software Interface",1998.
- 3. J.P. Hayes, "Computer Architecture and Organization", McGraw-Hill, 1998.
- 4. Recent literature in Computer Architecture and Organization.

COURSE OBJECTIVES

- To understand how computers are constructed out of a set of functional units and how the functional units operate, interact, and communicate.
- To make the students to understand the concept of interfacing memory and various I/O devices to a computer system using a suitable bussystem.

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)	
Apply the basic knowledge of digital concept to the functional components of a Computer System.	PO1,PO2,PO9	
1. Analyze the addressing mode concepts and design the instruction set Architecture.	PO2,PO3,PO9	
2. Identify the functions of various processing units within the CPU of a Computer System.	PO3,PO4,PO5	
3. Analyze the function of the memory management unit and create suitable memory interface to the CPU.	PO1,PO9,PO10	
4. Recognize the need for recent Bus standards and I/O devices.	PO2,PO3,PO5	

COURSE PLAN – PART II

COURSE OVERVIEW

Students get exposure to the fundamentals of computer architecture . Students will be taught about the internal flow of processing units ,fetching of instructions and memory organization. Students will understand I/O Devices, bus, interface concepts. Further they will be exposed to pipelining, firewall, flowchart & applications.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery	
1.	Week 1 3 Contact Hours	Function and structure of a computer, Functional components of a Computer, Interconnection of components		
2.	Week 2 3 Contact Hours	Performance of a computer, Machine instructions, Memory locations & Addresses	Lecture	
3.	Week 3 3 Contact Hours	Operands, addressing modes, Instruction formats, Instruction sets,	C&T/ PPT or any suitable mode	
4.	Week 4 3 Contact Hours	Instruction set architectures - CISC and RISC architectures,		
5.	Week 5 3 Contact Hours	Super scalar Architectures, fixed point and floating point operations, ALU		
	ASSESS	Descriptive type (Written)		
6.	Week 6 3 Contact Hours	Fundamental concepts, Control unit, Multiple bus organization, Hardwired control, Micro programmed control, Pipelining,	Lecture C&T/ PPT or any suitable mode	

7.	Week 7 3 Contact Hours Data hazards, Instruction hazards, Influence on instruction sets, Data path and control considerations, Performance considerations.			Lecture C&T/ PPT or any suitable mode					
	ASSESS	Assignment							
8.	Week 8 3 Contact Hours	Basic concepts, Semiconductor RAM memories, ROM, Speed - Size and cost, Memory Interfacing circuits							
9.	Week 9 3 Contact Hours	Cache memory, Improving cache performance, Memory management unit, Shared/Distributed Memory, Cache coherency in multiprocessor, Segmentation, Paging,		Lecture C&T/ PPT or any suitable mode					
10.	Week 10 3 Contact Hours	Concept of virtual memory, Address translation, Secondary storage devices,							
11.	ASSESSMENT III - 20 Marks				Descriptive type (Written)				
12.	Week 11 3 Contact Hours	Accessing I/O devices, Input/output programming, Interrupts, Exception Handling, DMA, Buses			Lecture				
13.	Week 12 3 Contact Hours	I/O interfaces- Serial port, Parallel port, PCI bus, SCSI bus, USB bus,		C&T/ PPT or any suitable mode					
14.	Week 13 3 Contact Hours	Firewall and Infini band, I/O peripherals							
15.	Week 14 3 Contact Hours	CPA - 20 Marks		Descriptive type (Written)					
16.	Week 15 3 Contact Hours	HND ASSESSMENT — 50 Morke		Descriptive type (Written)					
COUR	COURSE ASSESSMENT METHODS (shall range from 4 to 6)								
S.No.	Mode of Assessmen	t	Week/Date	Duration	% Weightage				
1	Assessment I (Descriptive)		2 nd week of February 2018	60 Minutes	20				
2	Assessment II (Assignment)		1 st week of March 2018	-	10				
3	Assessment III (Descriptive)		3 rd week of March 2018	60 Minutes	20				
4	CPA Compensation Assessment		2 nd week of April 2018	60 Minutes	20				
5	Final Assessment		4 th week of April 2018	180 Minutes	50				
COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be									

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings Anonymous feedback through questionnaire COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, , academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

- 1. All the students are advised to check their NITT WEBMAIL/group mail/suggested by the course faculty, class representative regularly. All the correspondence (schedule of classes/schedule of assessment/ course material/ any other information regarding this course) will be done through them only.
- 2. Queries (if required) to the course teacher shall only be emailed to the email id specified by the teacher.

ATTENDANCE

- 3. Attendance will be taken by the faculty in all the contact hours. Every student should maintain minimum of 75 % physical attendance in these contact hours along with assessment criteria to attend the end semester examination.
- 4. Any student, who fails to maintain 75% attendance need to appear for the compensation assessment (CPA). On successful completion of CPA Class along with assessment criteria will be eligible for attending the end semester examination.
- 5. Those students who have attendance lag and also missed any of the continuous assessments (CAs) with a valid reason can appear for CPA to get eligibility for writing the end semester examination as quoted in Pt. 2.
- 6. Students not having 75% minimum attendance at the end of the semester and also fail to attend CPA Classes have to take up REDO the course.

COMPENSATION ASSESSMENT

- 7. Attending all the assessments are MANDATORY for every student.
- 8. If any student is not able to attend any of the continuous assessments due to genuine reason, student is permitted to attend the compensation assessment (CPA) with 20% weightage.
- 9. Finally, every student is expected to score min(ClassAverage/2,Maximun Mark/3) in the total assessment (1, 2, 3, 4 and 5) to pass the course. Otherwise the student would be declared fail and 'F' grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.

ACADEMIC HONESTY & PLAGIARISM

- 1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any assessments is considered dishonest.
- 2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
- 3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
- 4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.
- 5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL INFORMATION

eg.: The Course Coordinator is available for consultation at times that are displayed on the coordinator's office notice board. Queries may also be emailed to the Course Coordinator directly at magayathri@nitt.edu

Course Faculty CC-Chairperson HOD Hot