NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE OUTLINE			
Course Title	Digital Circuits and Systems		
Course Code	ECPC14	**No. of Credits**	3
Department	Electronics and Communication Engg.	**Faculty**	Dr.R.Malmathanraj
Pre-requisites Course Code	-		
Course Coordinator(s) (if, applicable)	-		
Other Course Teacher(s)/Tutor(s) E-mail	rmathan@nitt.edu	**Telephone No.**	0431-2503323
Course Type	✓ **Core course**	**Elective course**	

COURSE OVERVIEW

Students are exposed to the design of digital circuits. The challenges in digital logic design is explored. Students will understand the basic concepts in memory.Also they learn about Flipflops and conventional circuits. The synchronous digital design and challenges in designing them is analysed.

COURSE OBJECTIVES

To introduce the theoretical and circuit aspects of digital electronics, this is the back bone for the basics of the hardware aspect of digital computers.

To learn about combinational circuits

To learn about sequential circuits.

To understand the basic concepts and design of synchronous digital design.

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned PO**
1. Apply the knowledge of Boolean algebra and simplification of Boolean expressions to deduce optimal digital networks.	PO1, PO2,PO4, PO5
2. Study and examine the SSI, MSI and Programmable combinational networks.	PO1, PO2,PO4, PO6, PO11

3.Study and investigate the sequential networks using counters and shift registers; summarize the performance of logic families with respect to their speed, power consumption, number of ICs and cost.	PO2, PO4, PO6 , PO 11,
4.Work out SSI and MSI digital networks given a state diagram based on Mealy and Moore configurations.	PO5, PO6,PO8
5. Code combinational and sequential networks using Verilog HDL.	PO5

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
1.	1st WEEK	Number theory, Boolean postulates and laws –De-Morgan's Theorem- Principle of Duality	Chalk and Talk, PPT
2.	2nd WEEK	Minterm – Maxterm - Sum of Products (SOP) Product of Sums (POS),Karnaugh map Minimization, Don't care conditions	Chalk and Talk, PPT
3.	3rd WEEK	Implementation of Boolean expression using Basic gatesImplementations of Logic Functions using NAND, NOR implementation	Chalk and Talk, PPT
4.	4th WEEK	Combinational Logic design Design procedure – Half adder – Full Adder- CLA– Half subtractor – Full subtractor	Chalk and Talk, PPT
5.	5th WEEK	Circuit Design using Multiplexer	Chalk and Talk, PPT
6.	6th WEEK	Memory- ROM - ROM organization - PROM – EPROM – EEPROM	Chalk and Talk, PPT
7.	7th WEEK	Sequential Circuits- Latches,Flip flops SR, JK, T,D Counters	Chalk and Talk, PPT
8.	8th WEEK	Registers	Chalk and Talk, PPT
9.	9th WEEK	Synchronous sequential circuits	Chalk and Talk, PPT

10.	10th WEEK	Moore and Mealy circuits	Chalk and Talk, PPT
11.	11th WEEK	Moore and Mealy circuits	Chalk and Talk, PPT
12.	12th WEEK	Hazards ,Verilog HDL	Chalk and Talk, PPT
13.	13th WEEK	Verilog HDL	Chalk and Talk, PPT
14.	14th WEEK	Verilog HDL	

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Test-I	On completion of 2nd unit	60 Minutes	20
2.	Assignment I	On completion of 2nd unit	-	5
3.	Test-II	On completion of 4th unit	60 Minutes	20
4.	Assignment II	On completion of 4th unit	-	5
5.	Attendance#	Every day attendance will be taken		10
6.	End Semester Exam	-	180 Minutes	40

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

1. Wakerly J F, "Digital Design: Principles and Practices, Prentice-Hall", 2nd Ed., 2002.
2. D. D. Givone, "Digital Principles and Design", Tata Mc-Graw Hill, New Delhi, 2003.
3. S.Brown and Z.Vranesic, "Fundamentals of Digital Logic with Verilog Design", Tata Mc-GrawHill, 2008.
4. D.P. Leach, A. P. Malvino, GoutamGuha, "Digital Principles and Applications" , Tata Mc-GrawHill, New Delhi, 2011.
5. John.M Yarbrough, Digital Logic Applications and Design, Thomson Learning, 2002.
6. Charles H.Roth. Fundamentals of Logic Design, Thomson Learning, 2003.
7. Thomas L. Floyd, Digital Fundamentals, 8th Edition, Pearson Education Inc, New Delhi, 2003

The attendance marks to be calculated as below

Attendance percentage	Marks
100%	10
99 % - 95 %	9
94 % - 90 %	8
89 % - 80 %	6
79 % - 75%	4
<75 %	0

COURSE EXIT SURVEY

1. Feedback from the students will be obtained from students as per Institute Policy.

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

CORRESPONDENCE

1. All the students are advised to come to the class regularly. All the correspondence (schedule of classes/ schedule of assignment/ course material/ any other information regarding this course) will be intimated in the class only.

ATTENDANCE

1.Attendance will be taken by the faculty. Every student should maintain minimum 75% physical attendance (on other duty will not be considered) in these contact hours along with assessment criteria to attend the end semester examination.
2. Any student who fails to maintain 75% need to re do the course.

ASSESSMENT& GRADING POLICY

1.Attending all theassessments are mandatory for every student.
2. Schedule for all the assessments will be intimated in class or through class committee meeting.
3. A retest or reexam will be given in case of illness or medical emergency (Institute Doctors Certificate is required) and only if the course faculty is notified in advance by phone or email.

4. The minimum marks for passing this course and grading pattern will adhere to the regulations of the Institute. Moreover Grading will be done relatively by considering the total marks secured by the students in all the assessments (two tests, two assignments Attendance and End semester Examination).
5. In order to award a passing grade E, every student is expected to score minimum of 35 marks as the total marks and should have appeared in the End semester examination. Otherwise the student will be declared Fail and F grade will be awarded.
6. At any case, CPA will not be considered as an improvement test.

ACADEMY HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations , assignments , looking or attempts to look at another students or bringing and using study materials in any form for copying during any assessment is considered as dishonest.
2. Tendering of information such as giving one's program, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of academic dishonesty will result in the loss of marks on that assessment. Additionally the name of the students will be reported to the Class Committee chair person and the Head of Department.
5. Students who honestly produce the ORIGINAL and OUTSTANDING WORK will be rewarded.

ADDITIONAL COURSE INFORMATION

FOR SENATE CONSIDERATION

Course Faculty R. Malmathanraj **-CC-Chairperson** B. Mahanty **HOD**