NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE OUTLINE TEMPLATE			
Course Title	DIGITAL ELECTRONICS LABORATORY		
Course Code	ECLR11	No.of Credits	1
Department	Electronics and Communication Engg.	Faculty	Dr.G. Thavasi Raja Mr. K.Gobinath
Pre-requisites Course Code	-		
Course Coordinator(s) (if, applicable)	-		
Other Course Teacher(s)/Tutor(s) E-mail	thavasi@nitt.edu	Telephone No.	0431-2503317
Course Type	✓ Core course	Elective course	

COURSE OVERVIEW

Digital Electronics Laboratory is a required course for freshman students in the ECE degree program. The purpose of the course is to provide students with an understanding of how to analyze, build, and troubleshoot digital circuits. Student should become proficient in using oscilloscopes, signal analyzers, and similar equipment to test digital circuits. In addition students must learn to write well-organized reports using a word processor. Students should also learn current technologies in the area of programmable memories.

COURSE OBJECTIVES

- To introduce basic postulates of Boolean algebra and shows the correlation between Boolean expressions
- To introduce the methods for simplifying Boolean expressions
- To outline the formal procedures for the analysis and design of combinational circuits and sequential circuits
- To learn combinational and sequentional circuit simulations using CAD tools.

COURSE OUTCOMES (CO)	
Course Outcomes	**Aligned Programme Outcomes (PO)**
1. Demonstrate theoretical device/circuit operation in properly constructed digital circuits.	PO1, PO2, PO4, PO6, PO10
2. Able to correctly operate standard electronic test equipment digital multi-meters, power supplies to analyze, test, and implement digital circuits.	PO1, PO2, PO4, PO6, PO10
3. Able to correctly analyze a circuit and compare its theoretical performance to actual performance.	PO1, PO2, PO4, PO6, PO10
4. Able to apply troubleshooting techniques to test digital circuits.	PO1, PO2, PO4, PO6, PO10
5. Able to code a given digital logic design in HDL language.	PO5, PO6, PO10

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
1.	I WEEK	1. Study of logic gates and verification of Boolean Laws.	Lab
2.	II WEEK	2. Design of adders and subtractors & code converters.	Lab
3.	III WEEK	3. Design of Multiplexers & Demultiplexers.	Lab
4.	IV WEEK	4. Design of Encoder and Decoder.	Lab
5.	V WEEK	5. 2bit and 8bit magnitude comparators	Lab
6.	VI WEEK	6. Study of flip-flops.	Lab
7.	VII WEEK	7. Design and implementation of counters using flip-flops	Lab
8.	VIII WEEK	8. Design and implementation of shift registers.	Lab
9.	IX WEEK	9. Simulation of adders, subtractors, encoders & decoder using CAD tools	Lab
10.	X WEEK	10. Simulation of counters & shift registers using CAD tools	Lab

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Evaluation during lab class	Every week (total 10 weeks)	15 mins	20
2.	Record work	To be submitted every next week after completion of experiment		5
3.	Quiz	One week prior to end semester	1 hour	25
4.	Lab attendance*			10
5.	Term Project	One week prior to end semester		10
6.	End semester evaluation		90 mins	30

*The assignment of marks for attetendance are given below.

Attendance %	Marks
100 %	10
95 %	8
90 %	6
85 %	4
80 %	2
< 80 %	0

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

1. John F.Wakerly, Digital Design, Fourth Edition, Pearson/PHI, 2006
2. John.M Yarbrough, Digital Logic Applications and Design, Thomson Learning, 2002.
3. Charles H.Roth. Fundamentals of Logic Design, Thomson Learning, 2003.
4. Donald P.Leach and Albert Paul Malvino, Digital Principles and Applications, 6th Edition, TMH, 2003.
5. Charles H. Roth, Jr., Lizy Kurian John Digital Systems Design Using VHDL, 2nd Edition, PWS Publishers, 1998.
6. Thomas L. Floyd, Digital Fundamentals, 8th Edition, Pearson Education Inc, New Delhi, 2003
7. Donald D.Givone, Digital Principles and Design, TMH, 2003
8. M. M. Mano, "Digital Design", 3rd ed., Pearson Education, Delhi, 2003.
9. Samir Palnitkar," Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Ed, Pearson Education Inc, New Delhi, 2001

COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

1. The students through class representative may give their feedback at any time which will be duly addressed.
2. Feedback from the students through MIS and class committee meetings

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

CORRESPONDENCE

1. All the students are advised to come to the class regularly. All the correspondence (schedule of classes/ schedule of assignment/ course material/ any other information regarding this course) will be intimated in the class only.

ATTENDANCE

1. Attendance will be taken by the faculty. 100 % is a mandatory. However, the relaxation upto 20% will be given for leave on medical, and other essential requirements followed in the institute. Every student should maintain minimum 80% physical attendance in these contact hours along with assessment criteria to attend the end semester examination.
2. Any student who fails to maintain 80% and misses any lab experiment needs to appear for the compensation classes with regular evaluation process. Students attendance is compulsory for Quiz and end semester.
3. Students not having 80% minimum attendance with compensation at the end of the semester will have to REDO the course.

ASSESSMENT

1. Attending all the assessments are mandatory for every student.
2. Please refer to B.Tech Regulations for the letter grades and corresponding grades.

Plagiarism, academic honesty: The students are expected to follow institute rules.

ADDITIONAL COURSE INFORMATION

Queries may also be emailed to the Course faculty directly at thavasi@nitt.edu.

FOR SENATE'S CONSIDERATION

(Dr. G. Thavasi Raja)
Course Faculty

CC-Chairperson (B. MALARKODI) HOD 21.07.2017.

K. GOBINATH.