DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE OUTLINE TEMPLATE			
Course Title	DEVICES AND NETWORKS LABORATORY		
Course Code	ECLR10	**No.of Credits**	1
Department	Electronics and Communication Engg.	**Faculty**	Mr.D.S.Roland Ms.R.Kiruthika
Pre-requisites Course Code	**ECPC11 & ECPC13**		
Course Coordinator(s) (if, applicable)	**Mr.D.S.Roland**		
Other Course Teacher(s)/Tutor(s) E-mail	kiruthikar@nitt.edu	**Telephone No.**	0431-2503334
Course Type	✓ **Core course**	**Elective course**	

COURSE OVERVIEW

Devices and Networks Laboratory intends to provide students a detailed understanding on the working principles and applications of the basic electronic active components like pn junction diodes, zener diodes, BJT and FET. Students will also get familiarized with variety of resistors and capacitors, power supplies, bench multimeters, oscilloscopes, waveform generators and bread boarding techniques. In addition, students will gain knowledge on basic analog circuits.

COURSE OBJECTIVES

- To understand the characteristics of pn junction diode.
- To understand the applications of zener diode.
- To obtain the input and output characteristics of CE transistor configuration using BJT and CS transistor configuration using JFET.
- To understand the operation of clipper and clamper circuits.
- To introduce basic filter circuits using passive components

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
1. Demonstrate theoretical device/circuit operation in properly constructed analog circuits.	**PO1, PO2, PO4, PO6, PO10**
2. Able to operate standard test equipment like multi-meters, oscilloscopes, power supplies, waveform generators, and to analyze, test, and implement circuits in breadboard.	**PO1, PO2, PO4, PO6, PO10**
3. Able to analyze the operation of an active device and compare its performance with the expected performance given in the data sheets.	**PO1, PO2, PO4, PO6, PO10**
4. Able to apply troubleshooting techniques to test the circuits.	**PO1, PO2, PO4, PO6, PO10**
5. Able to analyze the circuits using the simulation tools.	**PO5, PO6, PO10**

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
1.	I WEEK	1. Study of basic electronic components and equipments available in the lab.	Lab Exercise
2.	II WEEK	2. Study of the characteristics of PN Junction & Zener Diode as Regulator.	Lab Exercise
3.	III WEEK	3. Study the characteristics of Zener Diode and its application as Regulator.	Lab Exercise
4.	IV WEEK	4.Study of BJT characteristics using CE Configuration.	Lab Exercise
5.	V WEEK	5. Study of the Drain and Transfer characteristics of Field Effect Transistors.	Lab Exercise
6.	VI WEEK	6. Study the response of Series RLC Circuit.	Lab Exercise
7.	VII WEEK	7. Study the Constant K High pass Filters.	Lab Exercise

8. 9.	VIII WEEK IX WEEK	8. Design and implementation of Clippers and Clamper (Wave Shaping) Circuits. 9. Study the different types of Attenuators.	Lab Exercise Lab Exercise

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	**Observation**	**To be submitted every week while coming to the lab**		**25**
2.	**Record work**	**To be submitted every next week after completion of experiment**		**10**
3.	**Viva voce - Written Exam**	**One week prior to end semester**	**1 hour**	**40**
4.	**End semester evaluation**		**90 mins**	**25**

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

1. S.M. Sze, Semiconductors Devices, Physics and Technology, (2/e), Wiley, 2002.
2. A.S. Sedra & K.C. Smith, Microelectronic Circuits (6/e), Oxford, 2010.
3. L. Macdonald & A.C. Lowe, Display Systems, Wiley, 2003
4. J. Millman and C.C. Halkias: Electronic devices and Circuits, McGraw Hill, 1976.
5. Adir Bar-Lev: Semiconductors and Electronic Devices, (3/e), Prentice Hall, 1993.
6. B.G. Streetman, S.K. Banerjee: Solid state Electronic devices, (6/e), PHI, 2010.

COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

1. The students through class representative may give their feedback at any time which will be duly addressed.
2. Feedback from the students through MIS and class committee meetings.

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

CORRESPONDENCE

1. All the students are advised to come to the class regularly. All the correspondence (schedule of classes/ schedule of assignment/ course material/ any other information regarding this course) will be intimated in the class only.

ATTENDANCE

1. Attendance will be taken by the faculty. 100 % is a mandatory. However, the relaxation upto 20% will be given for leave on medical, and other essential requirements followed in the institute. Every student should maintain minimum 80% physical attendance in these contact hours along with assessment criteria to attend the end semester examination.
2. Any student who fails to maintain 80% and misses any lab experiment needs to appear for the compensation classes with regular evaluation process. Students attendance is compulsory for Quiz and end semester.
3. Students not having 80% minimum attendance with compensation at the end of the semester will have to REDO the course.

ASSESSMENT

1. Attending all the assessments are mandatory for every student.
2. No compensation assessment for Assessment 3 and 4.
3. Finally every student is expected to score minimum 1/3 rd of the top rank holder of the class (including all assessments) to pass the course. Otherwise student would be declared fail and 'F' grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.
4. Please refer to B.Tech Regulations 2015 for the letter grades and corresponding grades.

Plagiarism, academic honesty: The students are expected to follow institute rules.

FOR SENATE'S CONSIDERATION