NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI
Department of Electronics and Communication Engineering

Course Title	DSP Architecture		
Course Code	EC612	No. of Credits	3
Department	ECE	Faculty	Mrs.K.Akilandeswari
Pre-requisites Course Code	None		
Course Coordinator(s) (if, applicable)	-		
Other Course Teacher(s)/Tutor(s) E-mail	akilandeswari@nitt.edu	Telephone No.	0431-2503334
Course Type	✓ Elective course	☐ Core course	

COURSE OVERVIEW

This course provides the knowledge about various DSP architectures, their addressing modes and data formats. Students will be able to learn about On-chip peripherals, memory mapping and bus architectures of various DSP processors. They can acquire knowledge about real time implementation of applications like speech processing, video processing, biometrics etc.,

COURSE OBJECTIVE

To give an exposure to the various fixed point and floating point DSP architectures and to implement real time applications using these processors.

COURSE OUTCOMES (CO)

1. Learn the architecture details fixed and floating point DSPs

2. Infer about the control instructions, interrupts, and pipeline operations, memory and buses.

3. Illustrate the features of on-chip peripheral devices and its interfacing with real time application devices.

4. Learn to implement the signal processing algorithms and applications in DSPs.

5. Learn the architecture of advanced DSPs.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
1.	Week 1 (3 Contact Hours)	Fixed-point DSP architectures, TMS320C54X	Chalk &Talk, PPT or any suitable mode
2.	Week 2 (3 Contact Hours)	ADSP21XX , DSP56XX architecture details. Addressing modes. Control and repeat operations.	
3.	Week 3 (3 Contact Hours)	Interrupts. Pipeline operation. Memory Map and Buses.	
4.	Week 4 (3 Contact Hours)	TMS320C55X architecture and its comparison	
5.	Week 5 (3 Contact Hours)	Floating-point DSP architectures. TMS320C67X, DSP96XX architectures.	
6.	Week 6 (3 Contact Hours)	Cache architecture, Floating-point Data formats, On-chip peripherals	
7.	Week 7 (60 minutes)	**Assessment Exam -1 (Descriptive)**	Written Exam
	(1 Contact Hour)	Memory Map and Buses	Chalk &Talk, PPT or any suitable mode
8.	Week 8 (3 Contact Hours)	On-chip peripherals and interfacing, Clock generator with PLL, Serial port	
9.	Week 9 (3 Contact Hours)	McBSP. Parallel port. DMA. EMIF.	
10.	Week 10 (3 Contact Hours)	Serial interface- Audio codec, Sensors, A/D and D/A interfaces.	
11.	Week 11 (3 Contact Hours)	Parallel interface- RAM and FPGA, RF transceiver interface	
12.	Week 12 (60 minutes)	**Assessment Exam -II (Descriptive)**	Written Exam
	(2 Contact Hour)	DSP tools and applications. Implementation of Filters	Chalk &Talk,

13.	Week 13 (3 Contact Hours)	DFT, QPSK Modem, Speech processing, Video processing, Video Encoding / Decoding	PPT or any suitable mode
14	Week 14 (3 Contact Hours)	Biometrics. Machine Vision. High performance computing (HPC).	
15.	Week 15 (3 Contact Hours)	Digital Media Processors. Video processing sub systems	
16.	Week 16 (3 contact hours)	Multi-core DSPs. OMAP. CORTEX,	
	(60 minutes)	**Compensation Assessment**	
17.	**Week 17** (3 contact hours)	SHARC, SIMD, MIMD Architectures	
18.	**Week 18** (180 minutes)	**End Semester Exam**	**Descriptive type of exam**

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	ASSESSMENT-I (Descriptive)	13.02.2017 to 16.02.2017	60minutes	20
2.	ASSESSMENT-II (Descriptive)	20.03.2017 to 23.03.2017	60minutes	20
3.	Compensation Assessment (Descriptive)	3rd week of April 2017	60 minutes	20 (Refer Course Policy)
4.	Assignment / Seminar	3rd week of April 2017	-	10
5.	End semester (Descriptive type of exam)	1st week of May	180 minutes	50

ESSENTIAL READINGS :

Text Books

1. *B.Venkataramani&M.Bhaskar," Digital Signal Processor, Architecture, Programming and Applications",(2/e), McGraw- Hill,2010*
2. *S.Srinivasan&Avtar Singh, "Digital Signal Processing, Implementations using DSP Microprocessors with Examples from TMS320C54X", Brooks/Cole, 2004*

Reference Books

1. *S.M.Kuo&Woon-Seng S.Gan, "Digital Signal Processors: Architectures, Implementations, and Applications", Printice Hall, 2004.*
2. *N. Kehtarnavaz& M. Kerama, "DSP System Design using the TMS320C6000", Printice Hall, 2001.*
3. *S.M. Kuo&B.H.Lee,"Real-Time Digital Signal Processing, Implementations, Applications and Experiments with the TMS320C55X", John Wiley, 2001.*
4. *Recent literature in DSP Architecture.*

COURSE EXIT SURVEY

1. Feedback from the students during class committee meeting.

2. Queries through questionnaire.

COURSE POLICY

Correspondence: All the students are advised to come to class regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be intimated in class/ over phone/ in faculty room / through their webmail.
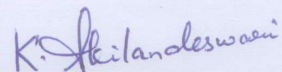
Attendance:

All the students should maintain minimum 75 % of physical attendance in these contact hours to attend the end semester exam. However, the relaxation will be given for leave on medical, and other essential requirements followed in the institute. Those who have less than 75% attendance can take up only FORMATIVE ASSESSMENT .

Assessment: Attending all the assessments is mandatory. Students absenting from any assessment(s), on genuine reason, may appear for compensation assessment (CPA) which will carry 20% weight. CPA cannot be considered as an improvement exam or as compensation for attendance.

ADDITIONAL COURSE INFORMATION

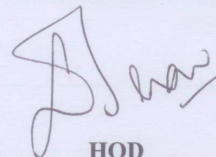Queries and feedback may also be emailed to the Course Faculty directly at akilandeswari@nitt.edu

FOR SENATE'S CONSIDERATION

Course Faculty	**PAC-Chairperson**	**HOD**