NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE OUTLINE TEMPLATE			
Course Title	SEMICONDUCTOR PHYSICS AND DEVICES		
Course Code	ECPC13	No. of Credits	03
Department	ECE – 2nd year 'A'	Faculty	S.RADHAKRISHNAN
Pre-requisites Course Code			
Course Coordinator(s) (if, applicable)			
Other Course Teacher(s)/Tutor(s) E-mail	srkrishnan@nitt.edu	Telephone No.	9629727495
Course Type	PC		

COURSE OVERVIEW

The course will focus on the physics of semiconductor devices and the principals of their operation. The initial parts of the courses will be used to establish a solid understanding of aspects of electrical conduction in semiconductors. The major part of the course will be focused on different applications of semiconductor like Diode, BJT, JFET & MOSFET. The use of transistor devices and their design and optimisation for integrated circuit applications will be presented in detail. Nanoscale transistor dimensions and the effect of such dimensions on transistor behavior will be presented. The physical limits to the scaling of CMOS devices will be discussed in detail.

COURSE OBJECTIVES

- To make the students understand the fundamentals of electronic devices.
- To train them to apply these devices in mostly used and important applications

COURSE OUTCOMES (CO)

COURSE OUTCOMES	Aligned Programme Outcomes (PO)
CO1: Deliver the concepts of basic semiconductor material physics and fabrication processes. CO2: Describe the characteristics of various electronic devices like diode, transistor etc., CO3: Classify and analyze the various circuit configurations of Transistor and MOSFETs. CO4: Illustrate the qualitative knowledge of Power electronic Devices. CO5: Describe the latest technological changes in Display Devices.	Students will be PO1: Apply the knowledge of basic semiconductor material physics and understand fabrication processes. PO2: Analyze the characteristics of various electronic devices like diode, transistor etc., PO3: Classify and analyze the various circuit configurations of Transistor and MOSFETs. PO4: Illustrate the qualitative knowledge of Power electronic Devices. PO5: Become Aware of the latest technological changes in Display Devices.

COURSE TEACHING AND LEARNING ACTIVITIES			
S.No.	**Week**	**Topic**	**Mode of Delivery**
1.	**July 11th ' 16 - July15th ' 16** (3 slots)	Crystal growth, film formation, lithography, etching and doping.	Lecture C&T/ PPT or any suitable mode
2.	**July 18th ' 16 - July 22nd '16** (3 slots)	Formation of energy bands in solids, Concept of hole, Intrinsic and extrinsic semiconductors	
3.	**July 25th ' 16 - July 29th ' 16** (3 slots)	Conductivity, Equilibrium Carrier concentration, Density of states and Fermi level	
4.	**Aug 01st ' 16 - Aug 05th ' 16** (3 slots)	Carrier transport – Drift and Diffusion, Continuity equation, Hall effect and its applications	
5.	**Aug 08th ' 16 - Aug 12th ' 16** (3 slots)	P-N junction diodes, Energy band diagram, biasing, V-I characteristics, Capacitances	
6.	**Aug 15th ' 16 - Aug 19th ' 16** (3 slots)	Diode models, Break down Mechanisms, Rectifiers, Limiting and Clamping Circuits	
7.	**Aug 22nd ' 16 - Aug 26th ' 16** (3 slots)	Types of diodes	
8.	**Aug 29th ' 16 - Sep 02nd ' 16** (3 slots)	BJT Physics and Characteristics modes of operation, Ebers-Moll Model	
9.	**Sep 05th ' 16 - Sep 09th ' 16** (3 slots)	BJT as a switch and Amplifier, Breakdown mechanisms, Photo devices	
10.	**Sep 12th ' 16 -Sep 16th ' 16** (3 slots)	MOSFET: Ideal I-V characteristics, non-ideal I-V effects	
11.	**Sep 19th ' 16 - Sep 23rd ' 16** (3 slots)	MOS Capacitor, MOSFET as switch, CMOS Logic gate Circuits, Bi-CMOS circuits, CCDs	
12.	**Sep 26th ' 16 - Sep 30th ' 16** (3 slots)	Power devices, operation and characteristics. Thyristor family	
13.	**Oct 03rd ' 16 - Oct 07th ' 16** (3 slots)	Power diodes. Power transistors	
14.	**Oct 10th ' 16 - Oct 14th ' 16** (3 slots)	Display devices, Operation of LCDs, Plasma, LED and HDTV	

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Assessment-I	2nd Week of Aug ' 16	60 Minutes	**25**
2.	Assessment-II	2nd Week of Sep ' 16	60 Minutes	**25**
3.	Assessment-III	4th Week of Oct ' 16	180 Minutes	**50**

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

Text Books

1. *S.M.Sze, Semiconductors Devices, Physics and Technology, (2/e), Wiley, 2002*
2. *A.S.Sedra&K.C.Smith, Microelectronic Circuits (5/e), Oxford, 2004*
3. *L.Macdonald&A.C.Lowe, Display Systems, Wiley, 2003*

Reference Books

1. *Robert Pierret, "Semiconductor Device Fundamentals," Pearson Education, 2006*
2. *J.Millman and C.C.Halkias: Electronic devices and Circuits, McGraw Hill, 1976.*
3. *B.G.Streetman: Solid state devices, (4/e), PHI, 1995.*
4. *N.H.E.Weste, D. Harris, "CMOS VLSI Design (3/e)", Pearson, 2005.*

Websites

1. Semiconductor Physics And Devices – ACM Digital Library
2. National Programme on Technology Enhanced Learning (NPTEL)

COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

Feedback from the students during class committee meetings

Anonymous feedback through questionnaire

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

CORRESPONDENCE

1. All the students are advised to check their NITT WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be intimated in Class Only.

ATTENDANCE

1. Attendance will be taken by the faculty in all the contact hours. Every student should maintain minimum 75 % physical attendance in these contact hours along with assessment criteria to attend the end semester examination.
2. Any student, who fails to maintain 75% attendance need to appear for the compensation assessment (CPA). Student who scores more than 60 % marks in the CPA along with assessment criteria will be eligible for attending the end semester examination.
3. Those students who have attendance lag and also missed any of the continuous assessments (CAs) can appear for CPA to get eligibility for writing the end semester examination as quoted in Pt. 2. Their scores in the CPA WILL NOT be taken into account for computing marks for CA.
4. Students not having 75% minimum attendance at the end of the semester and also fail in CPA (scoring less than 60%) will have to RE DO the course.

ASSESSMENT

1. Attending all the assessments are MANDATORY for every student.
2. If any student is not able to attend any of the Assessments due to genuine reason, student is permitted to attend the Repeat assessment (RA) with Corresponding weightage.
3. Student who fails to score 60% in RA will take up additional assignments to get eligibility for writing End Semester examination.
4. Finally, every student is expected to score minimum 1/3rd of the top rank holder of the class(Including all the assessments) to pass the course. Otherwise the student would be declared fail and 'F' grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.
5. Please refer B.Tech Regulations 2015(B.12.1) for the letter grades and the corresponding grades.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student's paper or bringing and using study material in any form for copying during any assessments is considered dishonest.
2. Tendering of information such as giving one's program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL COURSE INFORMATION

1. The faculty is available for consultation at times as per the intimation given by the faculty.
2. Queries (if required) to the course teacher shall only be emailed to the email id specified by the teacher(srkrishnan@nitt.edu)

FOR SENATE'S CONSIDERATION

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____ 4/7/2016