NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE PLAN – PART I			
Name of the programme and specialization	**B.TECH / CSE**		
Course Title	**Digital Laboratory**		
Course Code	CSLR32	**No. of Credits**	**2**
Course Code of Pre-requisite subject(s)	-	**Semester**	III
Session	July / ~~January~~ 2021	**Section (if, applicable)**	A
Name of Faculty	Dr. Bala Krishnan R	**Department**	CSE
Official Email	balakrishnan@nitt.edu	**Telephone No.**	-
Name of Course Coordinator(s) (if, applicable**)**	**NIL**		
Official E-mail	NIL	**Telephone No.**	NIL
Course Type (please tick appropriately**)**	**Minor Course**		

Syllabus (Approved in Senate)

Exercises

1. Verification of Boolean Theorems using basic gates.
2. Design and implementation of combinational circuits for arbitrary functions and code converters.
3. Design and implement Adder and Subtractor.
4. Implement Parity generator / checker.
5. Design and implement combinational circuits: 4 –bit binary adder / subtractor.
6. Design and implement shift-registers.
7. Design and implement synchronous and asynchronous counters.
8. Coding sequential circuits using HDL.
9. Coding combinational circuits using HDL.
10. Design of a 32-bit carry look-ahead adder with logarithmic depth using Verilog.
11. Design of a Wallace tree multiplier using Verilog.
12. Design and implementation of board using Verilog.

COURSE OBJECTIVES

1. To understand the overview on the design principles of digital computing systems
2. To learn Boolean Algebra and Understand the various logic gates
3. To develop programs in Hardware Description Language
4. To design and implement synchronous sequential, asynchronous sequential circuits
5. To be familiar with basic combinational and sequential components used in the typical data path designs

MAPPING OF COs with POs	
Course Outcomes	**Programme Outcomes (PO)** (Enter Numbers only)
1. Comprehend the digital design logic	1, 7
2. Design synchronous sequential circuits using basic flip-flops, counters, PLA, PAL	1, 3, 7
3. Design and develop basic digital systems	1, 5, 9, 12
4. Debug digital circuits	1, 3, 7, 12
5. Use boolean simplification techniques to design a combinational hardware circuit	1, 7

COURSE PLAN – PART II

COURSE OVERVIEW

This course covers data sciences, focusing on various concepts of machine learning. It provides details about some of the well-known supervised and unsupervised learning algorithms.

COURSE TEACHING AND LEARNING ACTIVITIES   (Add more rows)

Sl. No.	Week/Contact Hours	Topic	Mode of Delivery
1	03.08.2021 3 hours	Verification of Boolean Theorems using basic gates	Online
2	10.08.2021 3 hours	Design and implementation of combinational circuits for arbitrary functions and code converters	Online
3	17.08.2021 3 hours	Design and implement Adder and Subtractor	Online
4	24.08.2021 3 hours	Implement Parity generator / checker	Online
5	31.08.2021 3 hours	Design and implement combinational circuits: 4 –bit binary adder / subtractor	Online
6	14.09.2021 3 hours	Mid Exam 1	Online

7	21.09.2021 3 hours	Design and implement shift-registers	Online
8	28.09.2021 3 hours	Design and implement synchronous and asynchronous counters	Online
9	05.10.2021 3 hours	Coding sequential circuits using HDL	Online
10	12.10.2021 3 hours	Coding combinational circuits using HDL	Online
11	26.10.2021 3 hours	Mid Exam 2	Online
12	02.11.2021 3 hours	Design of a 32-bit carry look-ahead adder with logarithmic depth using Verilog	Online
13	09.11.2021 3 hours	Design of a Wallace tree multiplier using Verilog	Online
14	23.11.2021 3 hours	Design and implementation of board using Verilog	Online

COURSE ASSESSMENT METHODS (shall range from 4 to 6**)**

Sl. No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Continuous Assessment	Every Lab Session	3 hours	40
2	Mid Exam 1	Sep 3rd Week	90 minutes	15
3	Mid Exam 2	Oct 5th Week	90 minutes	15
4	End Semester Exam	Nov 4th Week	2 hours	30

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed**)**

1. **Students' feedback through PAC meetings**
2. **Feedbacks are collected before final examination through MIS or any other standard format followed by the institute**
3. **Students, through their Class Representatives, may give their feedback at any time to the course faculty which will be duly addressed.**

COURSE POLICY (including compensation assessment to be specified**)**

MODE OF CORRESPONDENCE (email/ phone etc)

Email, in-person – after 4.00 pm.

COMPENSATION ASSESSMENT POLICY

1. **One compensation assessment will be given after completion of Cycle Test 1 and 2 for the students those who are absent for any assessment due to genuine reason.**
2. **Compensatory assessments would cover the syllabus of Cycle tests 1 & 2**
3. **The prior permission and required documents must be submitted for absence signed by HoD/CSE.**

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

➢ At least 75% attendance in each course is mandatory.

➢ A maximum of 10% shall be allowed under On Duty (OD) category.

➢ Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

➢ Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.

➢ Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.

➢ The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

➢ The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION , IF ANY

TEXT BOOK

1. Morris Mano, Michael D. Ciletti, "Digital Design", Fifth Edition, PHI, 2012.
2. Samir Palnitkar, "Verilog HDL", Second Edition, Pearson Education, 2003.

REFERENCE BOOKS

1. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL", Second Edition, Pearson Education, 2010.
2. Stephen Brown, "Fundamentals of Digital Logic with Verilog", McGraw Hill, 2007.

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1. The Course Coordinator is available for consultation during the time intimated to the students then and there.
2. Relative grading adhering to the instructions from the office of the Dean (Academic) will be adopted for the course.

FOR APPROVAL

Course Faculty _____ CC-Chairperson _____ HOD _____