# NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

## DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

| COURSE PLAN – PART I | | | |
|---|---|---|---|
| **Name of the programme and specialization** | **B.Tech and CSE** | | |
| **Course Title** | **MICROPROCESSORS AND MICROCONTROLLERS** | | |
| **Course Code** | **CSPC36** | **No. of Credits** | **3** |
| **Course Code of Pre-requisite subject(s)** | **CSPC22** | **Semester** | **VI** |
| **Session** | **January 2020** | **Section (if, applicable)** | **A** |
| **Name of Faculty** | **Ms.A.Lavanya Mathiyalagi** | **Department** | **CSE** |
| **Official Email** | **lavanyaa@nitt.edu** | **Telephone No.** | **0431-2502202** |
| **Name of Course Coordinator(s)** (if, applicable) | **-** | | |
| **Official E-mail** | **-** | **Telephone No.** | **-** |
| **Course Type** | ✓ **Core course** | ☐ **Elective course** | |

**Syllabus (approved in Senate)**

**Unit – I**

**THE 8086 Microprocessor:** Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.

**Unit – II**

**8086 System Bus Structure:** 8086 signals – Basic configurations – System bus timing – System design using 8086 – IO programming – Introduction to Multiprogramming – System Bus Structure – Multiprocessor configurations – Coprocessor, Closely coupled and loosely Coupled configurations – Introduction to advanced processors.

**Unit – III**

**Microcontroller:** Architecture of 8051 – Special Function Registers(SFRs) - I/O Pins Ports and Circuits - Instruction set - Addressing modes -Programming 8051 Timers – Interfacing Microcontroller **-**Serial Port Programming - Interrupts Programming – LCD & Keyboard - External Memory Interface- Stepper Motor.

**Unit – IV Introduction to Embedded Systems:** Complex systems and microprocessors– Embedded system design process – Instruction sets preliminaries - ARM Processor – CPU: programming input and output supervisor mode, exceptions and traps – Co-processors- Memory system mechanisms – CPU performance

**Unit – V Embedded Computing Platform Design and Optimization:** The CPU Bus-Memory devices and systems–Designing with computing platforms – platform-level performance analysis - Components for embedded programs-Models of programs- Assembly, linking and loading – compilation techniques- Program level performance analysis – Software performance optimization – Analysis and optimization of program size- Program validation and testing.

**Text Books**

1. Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer Systems: The 8086 / 8088 Family - Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007

2. Mohamed Ali Mazidi, Janice GillispieMazidi, RolinMcKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", 2nd Edition, Pearson Education, 2011

3. Marilyn Wolf, "Computers as Components - Principles of Embedded Computing System Design", 3rd Edition "Morgan Kaufmann Publisher (An imprint from Elsevier), 2012

**COURSE OBJECTIVES**

- To understand the concepts of Architecture of 8086 microprocessor
- To understand the design aspects of I/O and Memory Interfacing circuits
- To understand the architecture and programming of ARM processor

**MAPPING OF COs with POs**

| Course Outcomes | Programme Outcomes (PO) |
|---|---|
| 1. Ability to design and implement programs on 8086 microprocessor | 1,3,6 |
| 2. Ability to design I/O circuits and Memory Interfacing circuits | 1,3,6 |
| 3. Ability to design and develop components of ARM processor | 1,3,6 |

## COURSE PLAN – PART II

**COURSE OVERVIEW**

- Microprocessors are used extensively in the design of any computing facility. It contains units to carry out arithmetic and logic calculations, fast storage in terms of registers and associated control logic to get instructions from memory and execute them. A number of devices can be interfaced with them to develop a complete system application.

- Microcontrollers are single chip computers, integrating processor, memory and other peripheral modules into a single System-on-Chip (SoC). Apart from input-output ports, the peripherals often include timers, data converters, communication modules, and so on.

| COURSE TEACHING AND LEARNING ACTIVITIES | | | |
|---|---|---|---|
| **S.No.** | **Week/Contact Hours** | **Topic** | **Mode of Delivery** |
| 1 | Week 1 | Introduction to 8086 and architecture | Presentation,Chalk & Talk |
| 2 | Week 1 | Addressing modes | Presentation,Chalk & Talk |
| 3 | Week 1 | Instruction set and assembler directives | Presentation,Chalk & Talk |
| 4 | Week 2 | Assembly language programming | Presentation,Chalk & Talk |
| 5 | Week 2 | Modular Programming | Presentation,Chalk & Talk |
| 6 | Week 2 | Linking and Relocation, Stacks | Presentation,Chalk & Talk |
| 7 | Week 3 | Procedures AND Macros | Presentation,Chalk & Talk |
| 8 | Week 3 | Interrupts and interrupt service routines | Presentation,Chalk & Talk |
| 9 | Week 3 | Byte and String Manipulation | Presentation,Chalk & Talk |
| 10 | Week 4 | 8086 signals AND Basic configurations | Presentation,Chalk & Talk |
| 11 | Week 4 | System bus timing, System design using 8086 | Presentation,Chalk & Talk |
| 12 | Week 4 | IO programming | Presentation,Chalk & Talk |
| 13 | Week 5 | Introduction to Multiprogramming | Presentation,Chalk & Talk |
| 14 | Week 5 | System Bus Structure | Presentation,Chalk & Talk |
| 15 | Week 5 | Multiprocessor configurations | Presentation,Chalk & Talk |
| 16 | Week 6 | Coprocessor, Closely coupled and loosely Coupled configurations | Presentation,Chalk & Talk |
| 17 | Week 6 | Introduction to advanced processors. | Presentation,Chalk & Talk |
| 18 | Week 6 | Architecture of 8051 | Presentation,Chalk & Talk |

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| 19 | Week 7 | Special Function Registers(SFRs) | Presentation,Chalk & Talk |
| 20 | Week 7 | I/O Pins Ports and Circuits | Presentation,Chalk & Talk |
| 21 | Week 7 | Instruction set, Addressing modes | Presentation,Chalk & Talk |
| 22 | Week 8 | Programming 8051 Timers | Presentation,Chalk & Talk |
| 23 | Week 8 | Interfacing Microcontroller | Presentation,Chalk & Talk |
| 24 | Week 8 | Serial Port Programming | Presentation,Chalk & Talk |
| 25 | Week 9 | Interrupts Programming, LCD & Keyboard | Presentation,Chalk & Talk |
| 26 | Week 9 | External Memory Interface, Stepper Motor | Presentation,Chalk & Talk |
| 27 | Week 9 | Complex systems and microprocessors | Presentation,Chalk & Talk |
| 28 | Week 10 | Embedded system design process | Presentation |
| 29 | Week 10 | Instruction sets preliminaries | Presentation |
| 30 | Week 10 | ARM Processor | Presentation |
| 31 | Week 11 | CPU: programming input and output supervisor mode | Presentation |
| 32 | Week 11 | Exceptions and traps, Co-processors | Presentation |
| 33 | Week 11 | Memory system mechanisms,CPU Performance | Presentation |
| 34 | Week 12 | Complex systems and microprocessors | Presentation |
| 35 | Week 12 | The CPU Bus, Memory devices and systems | Presentation |
| 36 | Week 12 | Designing with computing platforms | Presentation |
| 37 | Week 13 | Platform-level performance analysis | Presentation |
| 38 | Week 13 | Components for embedded programs, Models of programs | Presentation |
| 39 | Week 13 | Assembly, linking and loading, Compilation techniques | Presentation |

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|---|---|---|---|
| 40 | Week 14 | Program level performance analysis, Software performance optimization | Presentation |
| 41 | Week 14 | Analysis and optimization of program size, Program validation and testing | Presentation |

**COURSE ASSESSMENT METHODS**

| S.No. | Mode of Assessment | Week/Date | Duration | % Weightage |
|---|---|---|---|---|
| 1 | Cycle Test-1 | As Per Schedule | 1 hour | 20 |
| 2 | Cycle Test-2 | As Per Schedule | 1 hour | 20 |
| 3 | Assignment | 1st week of April | 2 weeks | 10 |
| CPA | Compensation Assessment | 2nd week of April | 1 hour | 20 |
| 4 | Final Assessment * | As Per Schedule | 3hours | 50 |

***Mantotary**

**COURSE EXIT SURVEY**

- Feedback is collected before every cycle test and after the end semester exam in the feedback forms through MIS.
- Suggestions from the students for incorporated for making the course more understanding and interesting.
- Students, through their class representative may give their feedback at any time to the course faculty which will be duly addresses.
- Students may also give their feedback during class committee meeting.

**COURSE POLICY**

**MODE OF CORRESPONDENCE**

- Email , phone or in person

**COMPENSATION ASSESSMENT**

- Retest will be conducted if there is any valid reason for the absentees of cycle test 1 or cycle test 2. The portions for retest will the portions for cycle test 1 and cycle test 2.

**ATTENDANCE POLICY** (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

**ACADEMIC DISHONESTY & PLAGIARISM**

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable for all the programmes.

**ADDITIONAL INFORMATION, IF ANY**

- Students can meet the faculty for discussion and queries at any time during working hours seeking prior appointment from the faculty through the representative.

**FOR APPROVAL**

| Course Faculty | CC- Chairperson | HOD |
|---|---|---|
| 25/11/20 | 27/11/2020 | 27/11/2020 |

## Guidelines

a) The number of assessments for any theory course shall range from 4 to 6.

b) Every theory course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.

d) The passing minimum shall be as per the regulations.

| B.Tech. Admitted in | | | | P.G. |
|---|---|---|---|---|
| 2018 | 2017 | 2016 | 2015 | |
| 35% or (Class average/2) whichever is greater. | | (Peak/3) or (Class Average/2) whichever is lower | | 40% |

e) Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

f) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

g) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.