NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE PLAN – PART I			
Name of the programme and specialization	B.Tech. (CSE)		
Course Title	Microprocessors and Microcontrollers		
Course Code	CSPC36	No. of Credits	3
Course Code of Pre-requisite subject(s)	CSPC22		
Session	January 2019	Section (if, applicable)	B
Name of Faculty	Ms. C. Nandhini	Department	CSE
Official Email	nandhinic@nitt.edu	Telephone No.	
Name of Course Coordinator(s) (if, applicable)			
Official E-mail		Telephone No.	
Course Type (please tick appropriately)	☑ Core course	☐ Elective course	

Syllabus (approved in Senate)

Unit I:

The 8086 Microprocessor: Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.

Unit – II:

8086 System Bus Structure: 8086 signals – Basic configurations – System bus timing – System design using 8086 – IO programming – Introduction to Multiprogramming – System Bus Structure – Multiprocessor configurations – Coprocessor, Closely coupled and loosely Coupled configurations – Introduction to advanced processors.

Unit – III:

Microcontroller: Architecture of 8051 – Special Function Registers(SFRs) - I/O Pins Ports and Circuits - Instruction set - Addressing modes -Programming 8051 Timers – Interfacing Microcontroller -Serial Port Programming - Interrupts Programming – LCD & Keyboard - External Memory Interface- Stepper Motor.

Unit – IV:

Introduction to Embedded Systems: Complex systems and microprocessors– Embedded system design process – Instruction sets preliminaries - ARM Processor – CPU: programming input and output supervisor mode, exceptions and traps – Co-processors- Memory system mechanisms – CPU performance.

Unit – V:

Embedded Computing Platform Design and Optimization: The CPU Bus-Memory devices and systems–Designing with computing platforms – platform-level performance analysis - Components for embedded programs-Models of programs- Assembly, linking and loading – compilation techniques- Program level performance analysis – Software performance optimization – Analysis and optimization of program size- Program validation and testing.

Text Books

1. Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer Systems: The 8086 / 8088 Family - Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007

2. Mohamed Ali Mazidi, Janice GillispieMazidi, RolinMcKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", 2nd Edition, Pearson Education, 2011

3. Marilyn Wolf, "Computers as Components - Principles of Embedded Computing System Design", 3rd Edition "Morgan Kaufmann Publisher (An imprint from Elsevier), 2012

COURSE OBJECTIVES

- To understand the concepts of Architecture of 8086 microprocessor
- To understand the design aspects of I/O and Memory Interfacing circuits
- To understand the architecture and programming of ARM processor

MAPPING OF COs with Pos

Course Outcomes	Programme Outcomes (PO) (Enter Numbers only)
1. Ability to design and implement programs on 8086 microprocessor	**1, 3, 6**
2. Ability to design I/O circuits and Memory Interfacing circuits	**1, 2, 4**
3. Ability to design and develop components of ARM processor	**1, 5, 7**

COURSE PLAN – PART II

COURSE OVERVIEW

- Microprocessors are used extensively in the design of any computing facility. It contains units to carry out arithmetic and logic calculations, fast storage in terms of registers and associated control logic to get instructions from memory and execute them. A number of devices can be interfaced with them to develop a complete system application.

- Microcontrollers are single chip computers, integrating processor, memory and other peripheral modules into a single System-on-Chip (SoC). Apart from input-output ports, the peripherals often include timers, data converters, communication modules and so on.

COURSE TEACHING AND LEARNING ACTIVITIES			
S.No.	**Week/Contact Hours**	**Topic**	**Mode of Delivery**
1	1/1	Introduction to 8086	Chalk and Board
2	1/2	Microprocessor Architecture, Addressing Modes	Chalk and Board, PPT
3	1/3	Instruction Set and Assembler directives	Chalk and Board, PPT
4	2/1	Assembly language programming	Chalk and Board, PPT
5	2/2	Assembly language programming	Chalk and Board, PPT
6	2/3	Modular programming	Chalk and Board, PPT
7	3/1	Linking and Relocation	Chalk and Board, PPT
8	3/2	Stacks, Procedures	Chalk and Board, PPT
9	3/3	Procedures, Macros	Chalk and Board, PPT
10	4/1	Interrupts and Interrupt service routines	Chalk and Board, PPT
11	4/2	Byte and String Manipulation	Chalk and Board, PPT
12	4/3	8086 Signals	Chalk and Board, PPT
13	5/1	Basic configuration, System bus structure	Chalk and Board, PPT
14	5/2	IO Programming	Chalk and Board, PPT
15	5/3	Multiprogramming	Chalk and Board, PPT
16	6/1	Multiprocessor configurations, Coprocessor	Chalk and Board, PPT
17	6/2	Closely coupled and Loosely coupled configurations	Chalk and Board, PPT
18	6/3	Introduction to advanced processor	Chalk and Board, PPT
19	6/3	Architecture of 8051	Chalk and Board, PPT
16	6/1	Special Function Registers	Chalk and Board, PPT
17	6/2	I/O pins, ports and circuits	Chalk and Board, PPT
18	6/3	Instruction set, addressing modes	Chalk and Board, PPT
19	7/1	Programming 8051 Timers	Chalk and Board, PPT
20	7/2	Interfacing Microcontroller, Serial port programming	Chalk and Board, PPT
21	7/3	Interrupts programming	Chalk and Board, PPT
22	8/1	LCD and Keyboard	Chalk and Board, PPT
23	8/2	External Memory Interface, Stepper Motor	Chalk and Board, PPT
24	8/3	Complex systems and microprocessors	Chalk and Board, PPT
25	9/1	Embedded system design process	Chalk and Board, PPT
26	9/2	Instruction set preliminaries	Chalk and Board, PPT
27	9/3	ARM Processor	Chalk and Board, PPT

28	10/1	CPU: Programming input and output	Chalk and Board, PPT
29	10/2	Supervisor mode, exceptions and traps	Chalk and Board, PPT
30	10/3	Co-processors	Chalk and Board, PPT
31	11/1	Memory system mechanisms	Chalk and Board, PPT
32	11/2	CPU performance	Chalk and Board, PPT
33	11/3	CPU bus and memory devices	Chalk and Board, PPT
34	12/1	Designing with computing platforms, Platform level performance analysis	Chalk and Board, PPT
35	12/2	Components for embedded programs, Models of programs	Chalk and Board, PPT
36	12/3	Assembly, linking and loading	Chalk and Board, PPT
37	13/1	Compilation techniques	Chalk and Board, PPT
38	13/2	Program level performance analysis	Chalk and Board, PPT
39	13/3	Software performance optimization	Chalk and Board, PPT
40	14/1	Analysis and optimization of program size	Chalk and Board, PPT
41	14/2	Program validation and testing	Chalk and Board, PPT

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Cycle Test-1	3rd week of Feb	1 hour	20
2	Assignment	2nd week of Mar	1 week	10
3	Cycle Test-2	1st week of Apr	1 hour	20
CPA	Compensation Assessment*	2nd week of Apr	1 hour	20
4	Final Assessment *	2nd week of May	3 hours	50

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Students through their class representative may give their feedback at any time to the course faculty which will be duly addressed. Students may also give their feedback during class committee meeting. Feedback questionnaire from students – from MIS at the end of the semester.

COURSE POLICY (including compensation assessment to be specified)

Students should not absent for assessments. If the reason for absence is genuine, the student can appear for compensation assessment. The medical certificate/on duty certificate should be submitted within one week after rejoining.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION, IF ANY

FOR APPROVAL

Course Faculty _____ **CC- Chairperson** _____ **HOD** 24/1/19

Guidelines

a) The number of assessments for any theory course shall range from 4 to 6.

b) Every theory course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.

d) The passing minimum shall be as per the regulations.

B.Tech. Admitted in				P.G.
2018	2017	2016	2015	
35% or (Class average/2) whichever is greater.		(Peak/3) or (Class Average/2) whichever is lower		40%

e) Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

f) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

g) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.