DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	Advanced Digital Design		
Course Code	CS616	**No. of Credits**	3
Course Code of Pre-requisite subject(s)	CSPC22 – Digital Systems Design		
Session	Jan. 2018	**Section (if, applicable)**	NA
Name of Faculty	Dr. N. Ramasubramanian	**Department**	CSE
Email	nrs@nitt.edu	**Telephone No.**	0431-2503204
Name of Course Coordinator(s) (if, applicable)	NA		
E-mail	NA	**Telephone No.**	NA
Course Type	Elective course		

Syllabus (approved in BoS)

Unit – I Review of Combinational and Sequential logic design – Structural models of combinational logic – Propagation delay – Behavioral Modeling – Boolean equation based behavioral models of combinational logic – Cyclic behavioral model of flip-flop and latches – A comparison of styles for behavioral modeling – Design documentation with functions and tasks

Unit – II Synthesis of Combinational and Sequential logic – Introduction to synthesis – Synthesis of combinational logic – Synthesis of sequential logic with latches – Synthesis of three-state devices and bus interfaces – Synthesis of sequential logic with flip-flops – Registered logic – State encoding – Synthesis of gated clocks and clock enables – Anticipating the results of synthesis – Resets – Synthesis of loops – Design traps to avoid – Divide and Conquer: partitioning a design.

Unit – III Design and Synthesis of Datapath Controllers – Partitioned sequential machines – Design example: Binary counter – Design and synthesis of a RISC stored-program machine – Processor, ALU, Controller, Instruction Set, Controller Design and Program Execution – UART – Operation, Transmitter, Receiver.

Unit – IV Programmable logic devices – Storage devices – Programmable Logic Array (PLA) – Programmable Array Logic (PAL) – Programmability of PLDs – Complex PLDs – Introduction to Altera and Xilinx FPGAs – Algorithms – Nested loop programs and data flow graphs – Design Example of Pipelined Adder, Pipelined FIR Filter – Circular buffers – FIFOs and Synchronization across clock domains – Functional units for addition, subtraction, multiplication and division – Multiplication of signed binary numbers and fractions.

Unit – V Postsynthesis Design Validation – Postsynthesis Timing Verification – Elimination of ASIC Timing Violations – False Paths – Dynamically Sensitized Paths – System Tasks for Timing Verificaion – Fault Simulation and Testing – Fault Simulation – Fault Simulation with Verifault-XL, lab exercises using Xilinx and Bluespec

Text Book

1. Michael D. Ciletti, "Advanced Digital Design with the VERILOG HDL, 2nd Edition, Pearson Education, 2010.

Reference Books

1. Samir Palnitkar "Verilog HDL", 2nd Edition, Pearson Education, 2003.
2. Stephenbrown, "Fundamentals of Digital Logic with Verilog", McGraw-Hill-2007.

COURSE OBJECTIVES

- To understand the basic building blocks, logic gates, adders, multipliers, shifters and other digital devices
- To apply logic minimization techniques for building digital systems
- To learn and to design using Hardware description language
- To understand the design of processors with examples

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
1. Ability to use standard digital elements for building a digital system	PO2, PO6
2. Ability to write programs using Verilog HDL for design of digital circuits	PO5, PO6
3. Ability to design complex digital systems using Verilog HDL	PO3, PO4, PO7
4. Ability to understand FPGAs and their application for digital system design	PO6, PO7

COURSE PLAN – PART II

COURSE OVERVIEW

Design and analysis of digital circuit using building blocks, timing in combinational and sequential circuits, programmable logic devices and RISC processor with arithmetic logic units,UART etc. An introduction to hardware description languages (HDL) such as Verilog and logic synthesis tools, which helps to develop the technical skills to design, simulate, analyze and verify complex digital circuits.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of
1	1/1	Review of Combinational and Sequential logic design	Chalk & Board
2	1/1	Structural models of combinational logic Propagation delay	Power Point
3	1/1	Behavioral Modeling Boolean equation based behavioral models of combinational logic	Power Point
4	2/1	Cyclic behavioral model of flip-flop and latches and A comparison of styles for behavioral modeling	Chalk & Board
5	2/1	Design documentation with functions and tasks	Chalk & Board

6	2/1	Synthesis of Combinational and Sequential logic – Introduction to synthesis and Synthesis of combinational logic	Power Point
7	3/1	Synthesis of sequential logic with latches and three-state devices and bus interfaces	Chalk & Board
8	3/1	Synthesis of sequential logic with flip-flops ,Registered logic and State encoding	Power Point
9	3/1	Synthesis of gated clocks and clock enables and Anticipating the results of synthesis along with Resets	Chalk & Board
10	4/1	Synthesis of loops , Design traps to avoid and Divide and Conquer : partitioning a design.	Chalk & Board
11	4/1	Design and Synthesis of Datapath Controllers Partitioned sequential machines and Design Example: Binary counter	Chalk & Board
12	4/1	Design and synthesis of a RISC stored-program machine for Processor, ALU, Controller,	Power Point
13	5/1	Instruction Set, Controller Design and Program Execution	Chalk & Board
14	5/1	Design Example UART –Operation, Transmitter, Receiver.	Chalk & Board
15	5/1	Programmable logic devices – Storage devices	--------
16	6/1	Programmable Logic Array (PLA) , Programmable Array Logic (PAL) , Programmability of PLDs and Complex PLDs	Chalk & Board
17	6/1	Introduction to Altera and Xilinx FPGAs	Chalk & Board
18	6/1	Algorithms , Nested loop programs and data flow graphs with Examples	---------
19	7/1	Design Example of Pipelined Adder and Pipelined FIR Filter	Chalk & Board
20	7/1	Circular buffers and FIFOs and Synchronization across clock domains	Chalk & Board
21	7/1	Functional units for addition, subtraction, multiplication and division	----------
22	8/1	Multiplication of signed binary numbers and fractions	Chalk & Board
23	8/1	Postsynthesis Design Validatio and Postsynthesis Timing Verification	Chalk & Board
24	8/1	Elimination of ASIC Timing Violations ,False Paths and Dynamically Sensitized Paths	----------
25	9/1	System Tasks for Timing Verificaion	Chalk & Board

26	9/1	Fault Simulation and Testing – Fault Simulation	Chalk & Board
27	9/1	Lab exercises using Xilinx.	--------
28	10/1	Fault Simulation with Verifault-XL,	Chalk & Board
29	10/1	Lab exercises using Xilinx.	Chalk & Board
30	10/1	Lab exercises using Bluespec	--------

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Cycle test 1	As per Schedule	1 Hr	20
2	Cycle test 2	As per Schedule	1 Hr	20
3	Assignment	1 week before final assessment	1 week	10
CPA	Compensation assessment	As per Schedule	1 Hr	20
4	Final Assessment *	As per Schedule	3 Hrs	50

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. Online feedback
2. Live feedback in the class

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, , academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

Email: nrs@nitt.edu / in person

ATTENDANCE

75% Attendance is mandatory

COMPENSATION ASSESSMENT

Students who are absent for Cycle test (for valid reasons only) should solve a set of tutorial problems and this will be evaluated for 20 marks. Prior permission from the faculty is required.

ACADEMIC HONESTY & PLAGIARISM

- Students should attend the classes sincerely and do more self learning
- Students should complete the assignments and lab exercises without doing any malpractice like copying, using bits etc.,

ADDITIONAL INFORMATION

Students can contact the faculty to clarify their doubts in person any time during working hours

FOR APPROVAL

Course Faculty Ranjani **CC-Chairperson** S. Selvakumar 31 01 18 **HOD** 31/1/2018