



**Department of Computer Science and Engineering  
National Institute of Technology Tiruchirappalli**

1. Course Outline			
<b>Course Title</b>	Computer Architecture		
<b>Course Code</b>	CSPC31		
<b>Department</b>	CSE	<b>No. of Credits</b>	4
<b>Pre-requisites Course Code</b>	CSPC24	<b>Faculty Name</b>	Mrs.A.Lavanya Mathiyalagi
<b>E-mail</b>	<a href="mailto:lavanyaa@nitt.edu">lavanyaa@nitt.edu</a>	<b>Telephone No.</b>	0431 – 2501801
<b>Course Type</b>	Core Course		

2.Course Overview
Computer Architecture helps to design complex modern microprocessors.
3. Course Objectives
<ul style="list-style-type: none"> <li>To understand the concept of advanced pipelining techniques</li> <li>To understand the current state of art in memory system design</li> <li>To know the working principle of I/O devices</li> </ul>
4. Course Outcomes (CO)
<ul style="list-style-type: none"> <li>Ability to apply performance metrics to find the performance of systems</li> <li>Ability to identify the problems in components of computer</li> <li>Ability to comprehend and differentiate various computer architectures and hardware</li> </ul>

5. Course Outcome (CO)	Aligned Programme Outcome (PO)							
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8
Ability to apply performance metrics to find the performance of systems	S	B	B	M	B	M	B	M
Ability to identify the problems in components of computer	S	B	M	B	B	M	B	B
Ability to comprehend and differentiate various computer architectures and hardware	M	B	B	B	M	S	B	M

S = 0.6

M = 0.4

B = 0.0

## 6. Course Teaching and Learning Activities

L.No	Title	Type		Mode of delivery			
		L	T	C & T	PP T	VL/VC	DEMO
<b>UNIT I</b>							
1.	Introduction	√		√			
2.	Classes of computers	√		√			
3.	Defining Computer Architecture	√		√			
4.	Trends in Technology	√		√			
5.	Trends in Power & Energy in Integrated Circuits	√		√			
6.	Trends in Cost	√			√		
7.	Dependability	√		√			
8.	Measuring, Reporting	√			√		
9.	Summarizing Performance	√		√			
10.	Quantitative Principles of Computer Design	√		√			
11.	Tutorial		√				
<b>UNIT II</b>							
12.	Basic and Intermediate pipelining Concepts	√		√			
13.	The Major Hurdle of Pipelining	√		√			
14.	Pipeline Hazards	√			√		
15.	Pipelining Implementation	√			√		
16.	Implementation issues that makes Pipelining hard	√		√			
17.	Extending the MIPS Pipeline to Handle Multicycle Operations	√		√			
18.	The MIPS R4000 Pipeline	√		√			
19.	Tutorial		√				
<b>UNIT III</b>							
20.	Instruction	√			√		
21.	Level Parallelism	√			√		
22.	Concepts and Challenges	√			√		
23.	Basic Compiler Techniques for Exposing ILP	√		√			
24.	Reducing Branch Costs with Prediction	√		√			
25.	Overcoming Data Hazards with Dynamic Scheduling	√		√			
26.	Dynamic Scheduling	√		√			
27.	Hardware-Based Speculation	√		√			
28.	Exploiting ILP Using Multiple Issue	√		√			
29.	Static Scheduling	√			√		
30.	Exploiting ILP	√			√		
31.	Advanced Techniques for Instruction Delivery and Speculation	√		√			

32.	Studies of the Limitations of ILP	√		√			
33.	Tutorial		√				
<b>UNIT IV</b>							
34.	Vector Architecture	√		√			
35.	SIMD Instruction Set Extensions for Multimedia	√		√			
36.	Graphics Processing Units	√		√			
37.	Detecting and Enhancing	√		√			
38.	Loop Level Parallelism	√			√		
39.	Centralized Shared Memory	√			√		
40.	Centralized Shared-Memory Architectures	√		√			
41.	Performance of Shared	√		√			
42.	Memory Multiprocessors	√		√			
43.	Distributed Shared Memory	√			√		
44.	Models of Memory Consistency	√		√			
45.	Multicore Processors and Their Performance	√		√			
46.	Tutorial	√		√			
<b>UNIT V</b>							
47.	Review of Memory Hierarchy Design	√		√			
48.	Cache Performance	√			√		
49.	Basic Cache Optimizations	√		√			
50.	Virtual Memory	√			√		
51.	Protection and Examples of Virtual Memory	√			√		
52.	Advanced Optimizations of Cache Performance	√		√			
53.	Memory Technology and Optimizations	√		√			
54.	Protection: Virtual Memory and Virtual Machines	√		√			
55.	Crosscutting Issues: The Design of Memory Hierarchies	√			√		
56.	Case Studies / Lab Exercises	√		√			
57.	Tutorial		√				

7. Course Assessment Methods				
Sl. No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assignment I	4 <sup>th</sup> Week of July'17	1 Week Time	5%
2	Cycle Test – 1	1 <sup>st</sup> Week of Aug'17	1 hour	20%
3	Assignment II	1 <sup>st</sup> Week of Sep'17	1 Week Time	5%
4	Cycle Test – 2	3 <sup>rd</sup> Week of Sep'17	1 hour	20%
5	End Semester Exam	2 <sup>nd</sup> Week of Nov'17	3 hours	50%
Total				100%

#### 8. Essential Readings (Textbooks, Reference books, Websites, Journals, etc.)

##### Text Books

1. David. A. Patterson and John L. Hennessy, "Computer Architecture: A Quantitative approach", Elsevier, 5<sup>th</sup> Edition, 2012

##### Reference Book

1. K. Hwang and Naresh Jotwani, "Advanced Computer Architecture, Parallelism, Scalability, Programmability", Tata McGraw Hill, 2<sup>nd</sup> Edition, 2010

9. Course Feedback Methods		
Feedbacks	Duration	Assesment method
I	1 <sup>st</sup> week of Aug'17	Offline through grade points (0 to 5)
II	2 <sup>nd</sup> week of Sep'17	
III	4 <sup>th</sup> week of Oct '17	

#### 10. Course Policy (including plagiarism, academic honesty, Attendance)

- **Attendance:** Minimum 75% is mandatory to write the end semester examination. Students having attendance 65%-74% are eligible for the end semester exam only after justifying their leave. Students have to redo the course, if they have less than 65% percentage of attendance at any cost. Students coming late to the class will not be provided attendance for that hour at any cost.
- Medical certificate or on-duty certificate should be submitted immediately after rejoining the next class.
- Students should turn off electronic devices during classes, such as cell phones, iPods, laptop, etc.
- **Academic Honesty:** Students disturbing the class, not attentive and students who do malpractices in assignments and test will not be permitted to attend any test commencing thereafter (including the end semester exam).
- Late submission of assignments will be awarded zero mark.

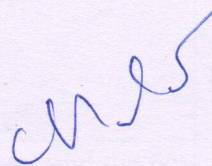
#### 11. Additional Course Information

Students can meet the faculty for discussion and queries at any time during working hours seeking prior appointment from the faculty through the class representative

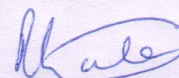
#### For Senate's consideration

A. Lavanya  
(A. Lavanya  
Mathiyalagi)

Course Faculty



Class Committee  
Chairperson



HOD