Department of Computer Science and Engineering
National Institute of Technology, Tiruchirappalli

1. Course Outline			
Course Title	**DIGITAL SYSTEMS DESIGN LABORATORY**		
Course Code	CSLR22		
Programme, Department & Section	B.Tech. – CSE B section	**No. of Credits**	3
Co-requisites Course Code	--	**Faculty Name**	S. Jaya Nirmala
E-mail	sjaya@nitt.edu	**Telephone No.**	0431 - 2503211
Course Type	ELR		
Session in Academic Year	July – November 2017 Session (Odd Semester)		

2.Course Overview

- This covers design and implementation of Digital circuits.

3. Course Objectives

- To develop programs in Hardware Description Language
- To design and implement synchronous sequential, asynchronous sequential circuits
- To be familiar with basic combinational and sequential components used in the typical data path designs

4. Course Outcomes (CO)

- Ability to design synchronous sequential circuits using basic flip-flops, counters, PLA, and PAL
- Ability to design and develop basic digital circuits
- Ability to debug digital circuits

5. Course Outcomes (CO)	Aligned Programme Outcome (PO)							
	PO-1	**PO-2**	**PO-3**	**PO-4**	**PO-5**	**PO-6**	**PO-7**	**PO-8**
Ability to design synchronous sequential circuits using basic flip-flops, counters, PLA, PAL	S	M	S	S	S	S	B	M
Ability to design and develop basic digital circuits	S	S	S	S	S	M	B	M
Ability to debug digital circuits	M	M	S	M	S	M	B	M

S = 0.6 M = 0.4 B = 0.0

6. Course Teaching and Learning Activities

S.No	Title	Type		Mode of delivery			
		L	T	C&T	PPT	VL/VC	DEMO
1	Study of Logic Gates	√					
2	Design of Adders						√
3	Design of Subtractors						√
4	Conversion of Binary to Excess-3						√
5	Design of Encoders and Decoders						√
6	Parity Generator and Checker						√
7	Design of a Multiplexor						√
8	Design of a Magnitute Comparator						√
9	Design of a Demultiplexor						√
10	Implementation of T, JK Flipflops						√
11	Conversion of Flip Flops						√
12	3-Bit Synchronous and Asynchronous Counter						√
13	Design and Implementation of Shift Registers						√
14	HDL Implementation of 4:1 Multiplexor						√
15	HDL Implementation of 4-Bit Full Adder						√
16	HDL Implementation of 4-Bit Ripple Counter						√

7. Course Assessment Methods

S. No.	Mode of Assessment	Week / Date	Duration	Marks
1	Continuous Assessment	Every Lab Session	3 hours	40
2	Record	Every Lab Session	-	10
3	Model Exam	6th Week	3 hours	25
4	End Semester Exam	2nd Week of November	3 hours	25
			Total	100

8. Essential Readings (Textbooks, Reference books, Websites, Journals, etc.)

1. *Morris Mano and Micheal D. Ciletti, "Digital System Design", 5th Edition, PHI, 2012*
2. *Samir Palnitkar, "Verilog HDL", 2nd Edition, Pearson Education, 2003*

7. Attendance

Students are expected to attend punctually all laboratory sessions. Minimum of 80% attendance is compulsory. Students registering late or who miss class are expected to make up all missed experiments in a manner determined by the faculty. Students should consult with their faculty about all class absences with proper proof (documentation required). It is the responsibility of the student to notify the faculty immediately about class absences and discuss any missed lab time, tests, or assignments. Extra classes will not be arranged.

For Senate's Consideration

Course Faculty	Class Committee Chairperson	HOD / CSE