NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

COURSE OUTLINE TEMPLATE			
Course Title	Advanced Digital Design		
Course Code	CS616	No. of Credits	3
Department	CSE	Faculty	Dr. N. Ramasubramanian
Pre-requisites Course Code	NIL		
E-mail	nrs@nitt.edu	Telephone No.	0431-2503204
Course Type	☐ Core course	☑ Elective course	

COURSE OVERVIEW

Advanced digital design course gives a review of switching algebra and combinational design, programmable logic devices, and combinational. Sequential circuits using latches, flip-flops, ROM and RAM and also reviewed. Topics in sequential circuit design are treated, including finite state machines, Mealy and Moore models, state diagrams and state tables, optimization, asynchronous sequential circuits, and races and hazards.

COURSE OBJECTIVES

- To understand the basic building blocks, logic gates, adders, multipliers, shifters and other digital devices
- To apply logic minimization techniques, including Karnaugh Maps
- To learn techniques and tools for programmable logic design

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
• Students understand the use standard digital memory devices as components in complex subsystems	PO- 1
• Technical know how to design simple combinational logic circuits and logic controllers	PO-1, PO-6
• Acquire skill set to develop the necessary software for basic digital systems	PO-8

COURSE TEACHING AND LEARNING ACTIVITIES			
S. No.	**Week**	**Topic**	**Mode of Delivery**
1	1	Review of Combinational circuit design	Pen-Board
2	1	Sequential logic design.	Pen-Board
3	1	Structural models of combinational logic Propagation delay	Pen-Board
4	2	Behavioral Modeling Boolean equation based behavioral models of combinational logic	Pen-Board
5	2	Cyclic behavioral model of flip-flop and latches	PPT
6	2	A comparison of styles for behavioral modeling	PPT
7	3	Design documentation with functions and tasks	PPT
8	3	Introduction to synthesis and Synthesis of combinational logic	PPT
9	3	Synthesis of sequential logic with latches	PPT
10	4	Three-state devices and bus interfaces	PPT
11	4	Synthesis of sequential logic with flip-flops	PPT
12	4	Registered logic and State encoding	PPT
13	5	Synthesis of gated clocks and clock enables and Anticipating the results of synthesis along with Resets	PPT
14	5	Synthesis of loops, Design traps to avoid and Divide and Conquer : partitioning a design	PPT
15	5	Design and Synthesis of Datapath Controllers	PPT
16	6	Partitioned sequential machines and Design Example: Binary counter	PPT
17	6	Design and synthesis of a RISC stored-program machine for Processor, ALU, Controller	PPT
18	6	Instruction Set, Controller Design and Program Execution	PPT
19	7	Design Example UART – Operation, Transmitter, Receiver.	PPT
20	7	Programmable logic devices	PPT
21	7	Storage devices	PPT

22	8	Programmable Logic Array (PLA) , Programmable Array Logic (PAL)	PPT
23	8	Programmability of PLDs and Complex PLDs	PPT
24	8	Introduction to Altera and Xilinx FPGAs	PPT
25	9	Algorithms, Nested loop programs	PPT
26	9	data flow graphs with Examples	PPT
27	9	Design Example of Pipelined Adder and Pipelined FIR Filter	PPT
28	10	Circular buffers and FIFOs and Synchronization across clock domains	PPT
29	10	Functional units for addition, subtraction, multiplication and division	PPT
30	10	Multiplication of signed binary numbers and fractions	PPT
31	11	Postsynthesis Design Validation and	PPT
32	11	Postsynthesis Timing Verification	PPT
33	11	Elimination of ASIC Timing Violations	PPT
34	12	False Paths and Dynamically Sensitized Paths	PPT
35	12	System Tasks for Timing Verification	PPT
36	12	Fault Simulation and Testing – Fault Simulation	PPT
37	13	Lab exercises using Xilinx.	PPT
38	13	Fault Simulation with Verifault-XL	PPT
39	13	Lab exercises using Xilinx.	PPT
40	13	Lab exercises using Bluespec	PPT

COURSE ASSESSMENT METHODS				
S.No	**Mode of Assessment**	**Week/Date**	**Duration**	**% Weightage**
1.	Cycle Test I	As per Academic Schedule	1 Hr	20%
2.	Cycle Test II	As per Academic Schedule	1 Hr	20%
3.	Assignment	Before End Sem Exam	~1 Week	10%
4.	End Sem Exam	As per Academic Schedule	3 Hrs	50%

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

1. Michael D. Ciletti, "Advanced Digital Design with the VERILOG HDL, 2nd Edition, Pearson Education, 2010.
2. Samir Palnitkar "Verilog HDL", 2nd Edition, Pearson Education, 2003.
3. Stephenbrown, "Fundamentals of Digital Logic with Verilog", McGraw-Hill-2007.

COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

On-line Feedback
Live Feedback in class

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

Academic honesty
Attendance Minimum 75% Mandatory

ADDITIONAL COURSE INFORMATION

Students can meet faculty for discussion and queries any time during working hours.

FOR SENATE'S CONSIDERATION

Course Faculty _____ CC-Chairperson 3/1/17 HOD 3/1/2017