NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE OUTLINE TEMPLATE			
Course Title	DIGITAL SYSTEMS DESIGN		
Course Code	CSPC22	**No. of Credits**	03
Department	CSE	**Faculty Name**	R.LEELA VELUSAMY / B. SHAMEEDHA BEGUM
Pre-requisites Course Code	-		
E-mail	leela@nitt.edu shameedha@nitt.edu	**Telephone No.**	0431-2503201 / 0431-2503215
Course Type	Core course		

COURSE OVERVIEW

This course has two main goals: (1) to teach students how a digital computer works and (2) to introduce students to verilog programming. The hardware component of the course begins by introducing the basic switching components of all digital circuits. It next shows how to analyze circuits and also how to build circuits that conform to specified computational properties. It introduces many standard circuits used by all computers, such as logic and shift circuits, arithmetic circuits, and memory circuits. The software part of this course explores the design aspects involved in the realization of CMOS integrated circuits/systems from device up to the register/subsystem level. It addresses major design methodologies with emphasis placed on structured full custom design. The course includes the study of the MOS device, critical interconnect and gate characteristics that determine the performance of VLSI circuits. This course will held the students to learn basic digital VLSI design paradigms and the necessary Verilog HDL constructs that would help them to build combinational & sequential logic circuits in CMOS.

COURSE OBJECTIVES

1. To understand the essential knowledge on the fundamentals and applications of digital circuits and digital computing principles.

2. To use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnects.

3. To understand of the characteristics of CMOS circuit construction.

4. To complete a significant VLSI design project having a set of objective criteria & design constraints.

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)							
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8
1. An ability to understand the functions of various hardware components and their building blocks.	S	M	S	M	M	S	B	M
2. An ability to understand the Boolean algebraic expressions to digital design.	S	M	M	B	B	M	B	S
3. Ability to design and implement complicated digital systems using Verilog.	S	S	S	S	S	S	B	S

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
		Unit – 1	
1.	1st (11.7.16 to 15.7.16)	Introduction to Digital Sytems, Binary codes, Weighted and non-weighted, Binary arithmetic conversion algorithms,Canonical and standard boolean expressions	Chalk and Talk
2.	2nd (18.7.16 to 22.7.16)	Truth tables, K-map reduction ,Don't care conditions. Adders,Subtractors ,Carry look-ahead adder.	Chalk and Talk
3.	3rd (25.7.16 to 29.7.16)	Code conversion algorithms ,Design of code converters , Equivalence functions.	Chalk and Talk
		Unit – 2	Chalk and Talk
4.	4th (01.8.16 to 02.8.16)	Binary/Decimal Parallel Adder/Subtractor for signed number,Magnitude comparator, Decoders Encoders.	Chalk and Talk

5.	5th (11.8.16 to 12.8.16)	Multiplexers / Demultiplexers - Boolean function implementation using multiplexers,Problems	
		Unit – 3	
6.	6th (15.8.16 to 19.8.16)	Introduction to Sequential logic - Basic latch -Flip-flops (SR, D, JK, T and Master-Slave) - Triggering of flipflops - Counters - Design procedure	Chalk and Talk
7.	7th (22.8.16 to 26.8.16)	Ripple counters ,BCD and Binary	Chalk and Talk
8.	8th (22.8.16 to 26.8.16)	Synchronous counters, Problems, Introduction to registers	Chalk and Talk
9.	9th (29.8.16 to 2.9.16)	Shift registers ,Registers with parallel load	Chalk and Talk
10.	10th (6.9.16 to 9.9.16)	Reduction of state and flow tables ,Race-free state assignment , Hazards.	Chalk and Talk
		Unit – 4	
11.	11th (12.9.16 to 16.9.16)	Introduction to VLSI design - Basic gate design , Digital VLSI design ,Design of general boolean circuits using CMOS gates	Chalk and Talk
12.	12th (12.9.16 to 16.9.16)	Introduction to Verilog Concepts – Basic concepts	PPT, Chalk and Talk
13.	13th (19.9.16 to 23.9.16)	Modules & ports & Functions	PPT, Chalk and Talk

14.	14th (26.9.16 to 30.9.16)	Useful modeling techniques	PPT, Chalk and Talk
15.	15th (3.10.16 to 7.10.16)	Timing and delays , user defined primitives	PPT, Chalk and Talk
		Unit – 5	
16.	16th (10.10.16 to 14.10.16)	Advanced Verilog Concepts , Synthesis concepts ,Inferring latches and flipflops	PPT, Chalk and Talk
17.	17th (17.10.16 to 21.10.16)	Modeling techniques for efficient circuit design. Design of high-speed arithmetic circuits	PPT, Chalk and Talk
18.	18th (24.10.16 to 28.10.16)	Parallelism Pipelined Wallace tree tipliers, Systolic algorithms, Systolic matrix multiplication	PPT, Chalk and Talk
19.	19th (12.9.16 to 16.9.16)	Problems and Discussion	Chalk and Talk

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Assignment	3rd Week	-	5%
2.	Cycle Test-1	3.8.16-10.8.16	1 Hr.	20%
3.	Assignment	6th Week	-	5%
4.	Cycle Test-2	9.11.16-16.11.16	1 Hr.	20%
5.	Semester Exam	16.11.16-25.11.16	3 Hrs.	50%

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

Text Books

1. Morris Mano and Michael D. Ciletti, "Digital Design", 5 th edition, Prentice Hall of India, 2012
2. Samir Palnitkar, "Verilog HDL", 2nd Edition, Pearson Education, 2003

Reference Books

1. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL, 2nd Edition, Pearson Education, 2010
2. Stephen Brown, "Fundamentals of Digital Logic with Verilog", McGraw Hill, 2007

COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

Student's Feed back report

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

Participation in class discussion is strongly encouraged.
Please turn off electronic devices during classes, like cell phones, iPods, Laptops, iPads, and iPhones.

FOR SENATE'S CONSIDERATION

Course Faculty : R. LEELA VELUSAMY B. SHAMEEDHA BEGUM

CC-Chairperson : N. RAMASUBRAMANIAN

HOD : R. LEELA VELUSAMY