Department of Computer Applications
National Institute of Technology Tiruchirappalli

1.Course Outline			
Course Title	Computer Organization and Architecture		
Course Code	CAS763		
Department	CA	**No. of Credits**	3
Pre-requisites Course	Knowledge of fundamentals of Digital Computers	**Faculty Name**	Dr.S.Domnic
PAC Chairman	Dr.S.Sangeetha		
E-mail	domnic@nitt.edu	**Telephone No.**	0431-2503745
Course Type	Core Course		

2. Course Overview

The Computer Organization and Architecure course deals with the design principles and various organizational issues of a Digital Computer. Various binary systems for representing information in digital systems, binary arithmetic operations, Boolean algebra, logic gates used in the design of digital systems, simplification of Boolean expressions using map method will be discussed. The procedures for the analysis and design of combinational and sequential circuits will be explained. The components of the computer system such as processor, memory and I/O modules and interconnection of these components will be dealt. The architectural issues such as instruction set design and organization issues such as piplenining will be dealt. Further, various processor technologies will also be taught.

3. Course Objectives

- To understand the basic structure of a digital computer
- To study the operations of internal components

4. Course Outcomes (CO)

Students will be able to:

- Define the Boolean algebra and explain its use in circuit design
- List the different types of memory and distinguish them
- Discriminate the various functional units of CPU and illustrate functioning of I/O devices
- Explain latest processor technologies and evaluate systems for one’s own requirements

5. Course Outcome (CO)	Aligned Programme Outcome (PO)											
	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12
Define the Boolean algebra and explain its use in circuit design	S	S	S	M	M	B	B	B	B	B	B	B
List the different types of memory and distinguish them	S	M	S	M	M	B	B	M	B	B	B	B
Discriminate the various functional units of CPU and illustrate functioning of I/O devices	S	M	B	M	M	B	M	B	B	B	B	B
Explain latest processor technologies and evaluate systems for one's own requirements	S	M	M	M	M	B	S	B	B	B	B	M

S = 0.6 M = 0.4 B = 0.0

6. Course Teaching and Learning Activities

Week	Mode of Delivery	Topics covered
1.	Class-I	Introduction – Computer organization – Computer architecture
	Class-II	Number systems –Number-Base conversions
	Class-III	Singed binary number – binary arithmetic - complements
2.	Class-I	Boolean algebra – basic theorems and properties
	Class-II	Boolean functions - gates
	Class-III	Simplification of Boolean functions using algebraic method
3.	Class-I	Canonical and standard forms
	Class-II	Map simplifications – two, three and four variable maps
	Class-III	Don't-care conditions – gate representation(NAND & NOR)
4.	Class-I	Combinational circuits – binary adder-subtractor
	Class-II	binary multiplier – magnitude comparator
	Class-III	Decoders – encoders – multiplexers – demultiplexer
5.	Class-I	Sequential cirucuits – latches – flipflops – registers – shift registers
	Class-II	Counters – ripple counters – synchronous counters
	Class-III	Internal memory – semiconductor main memory
6.	Class-I	External memory – magnetic disk
	Class-II	RAID

Week	Mode of Delivery	Topics covered
	Class-III	Optical memory - Magnetic tape
7.	Class-I	virtual memory
	Class-II	Cache memory
	Class-III	CPU – Arithmetic and logic unit
8.	Class-I	Instruction sets
	Class-II	Instruction sets
	Class-III	Instruction cycle – addressing modes
9.	Class-I	Addressing modes and formats
	Class-II	Instruction pipelining
	Class-III	Processor organization – register organization
10.	Class-I	Control unit operation
	Class-II	External devices – I/O modules
	Class-III	Programmed I/O
11.	Class-I	Interrupt driven I/O
	Class-II	Direct memory access
	Class-III	I/O channels and processors
12.	Class-I	Asynchronous data transfer
	Class-II	Reduced Instruction Set Computers, Complex Instruction Set Computers
	Class-III	Superscalar processor
13.	Class-I	Vector processor
	Class-II	Parallel processor – cluster processor
	Class-III	Distributed, Embedded and MultiCore processors

The assessment for this theory paper consists of two cycle tests, assignment and end semester examination. The final marks will be computed for a total of 100.

7. Course Assessment Methods – Theory				
Sl. No.	**Mode of Assessment**	**Week/Date**	**Duration**	**Weightage(%)**
1.	Cycle Test – 1	6^{th} week	60 Mins	20
2.	Cycle Test – 2	10^{th} week	60 Mins	20
3.	Assignment-1 and Assignment-2	5^{th} week and 9^{th} week		10
4.	End Semester Exam	-	180 Mins	50
			Total	100

8. Essential Readings (Textbooks, Reference books, Websites, Journals, etc.)

Books

1. M. Morris Mano and Michael D. Ciletti, Digital Design, 4 Edn, 2007, Pearson.
2. William Stallings, "Computer Organization and Architecture", 7 Edn., 2006, PHI.
3. Hayes, J.P. "Computer Architecture and Organization", 3 Edn., 1998, McGraw Hill.

9. Course Exit Survey (mention the ways by which the feedback about the course is assessed and indicate the attainment level)

- The students through the class rep may give their feedback at any time to the course co-ordinator which will be duly addressed.
- The students may also give their feedback during Class Committee meeting.

10. Course Policy (including plagiarism, academic honesty, attendance, etc.)

- **Plagiarism**
  The students are expected to not do malpractice in cycle tests/examinations. If found to copy from bits/other students, action will be taken.
- **Attendance**
  100% is a must. However, relaxation upto 25% will be given for leave on emergency requirements (medical, death, etc.) and representing institute events.
- **Academic Honesty**
  i) Possession of any electronic device, if any, found during the test or exam, the student will be debarred for 3 years from appearing for the exam and this will be printed in the Grade statement/Transcript.
  ii) Tampering of MIS records, if any, found, then the results of the student will be with heldand the student will not be allowed to appear for the Placement interviews conducted by the Office of Training & Placement, besides (i).

11. Additional Course Information

- The students can get their doubts clarified at any time with their faculty member with prior appointment.

For Senate's Consideration

Dr.S.Domnic
Course Faculty

(Dr. S. Sangeetha)
PAC Chairperson

S.R.Balasundaram
(Dr. S.R.Balasundaram)
HoD